HONOR CODE

- I have not used any online resources during the exam.
- I have not obtained any help either from anyone in the class or outside when completing this exam.
- No sharing of notes/slides/textbook between students.
- NO SMARTPHONES.
- **CANVAS ANSWERS WILL BE LOCKED AFTER 1ST TRY.**

Questions Sheet.

Read all of the following information before starting the exam:

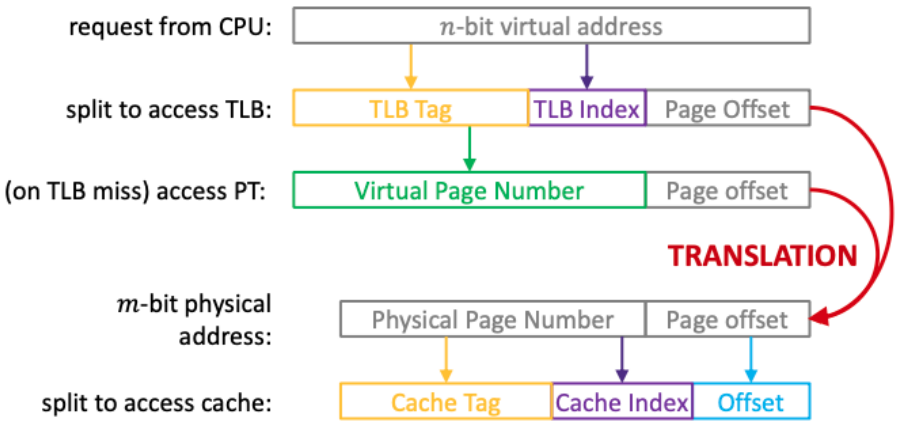
- For each question fill out the appropriate choice. If no text box is provided, you do not need to fill out written text.
- Show all work, clearly and in order, if you want to get full credit.
- I reserve the right to take off points if I cannot see how you logically got to the answer (even if your final answer is correct).
- Circle or otherwise indicate your final answers.
- Please keep your written answers brief; be clear and to the point.
- I will take points off for rambling and for incorrect or irrelevant statements. This test has six problems.

- HONOR CODE
- Questions Sheet.
- Section Virtual Memory 22 points. Canvas Q1-Q22
  - Common questions. Canvas Q1-Q2
  - For the virtual address 0x2cade0 answer the following Canvas Q3-Q12
  - For the virtual address 0x301754 answer the following. Canvas Q13-Q22
- B. Section Cache I Questions. 15 points. Canvas Q23-Q25
  - 23. What is the miss rate for loop 1? (Assume that only loop 1 runs). 5 points
  - 24. What is in the cache at the end of loop 1? 5 points
  - 25. What is the miss rate for loop 2 ? Assume that loop 1 has already run to completion and has warmed up the cache. 5 points
- C. Section Cache II Questions. 20 points. Canvas Q26-Q31
  - 26. Assuming the total size of the physical address is 32 bits. What is the number of bits required by tag, index and offset (4 points)
  - 27. What is the hit rate of this direct-mapped cache? (4 points)
  - 28. What type of misses occur (Conflict, Compulsory, Capacity) ? (2 points)
  - 29. What is the hit rate a 2-way set associative cache. 512 bytes. 8 words/block. (4 points)
  - 30. What type of misses occur (Conflict, Compulsory, Capacity) in the 2-way cache ? (2 points)
  - 31. Now consider a 4-way set associative cache. 512 bytes. 8 words/block.What is the hit rate ? (4 points)
- D. RISC-V Pipeline 20 points. Canvas Q32-Q41
  - 32. In which cycle does `addi x18,x0,0` (instruction 2) run the EX stage ?
  - 33. In which cycle does `beq x9,x18,exit` (instruction 3) read the registers?
  - 34. In which cycle does the `lw x9, 10(x8)` (instruction 4) start the IF stage ?
  - 35. In which cycle does the `lw x9, 10(x8)` read the registers ?
  - 36. In which cycle does the `xor x9, x9, x18` (instruction 5) reach the IF stage ?
  - 37. In which cycle does the `xor x9,x9,x18` (instruction 5) read the registers ?
  - 38. In which stage is `sw x9, 10(x8)` stalled and how many cycles?
  - 39. In which cycle does the `sw x9, 10(x8)` (instruction 6) write the memory location ?
  - 40. How many instructions are stalled due to data hazards ?
  - 41. How many cycles do we have stall in total for this program ? i.e., Consider a program with 6 instruction and no hazards and ran to completion in T cycles. This program completed in T_hazard cycles. What is (T_hazard - T)?
- E. RISC-V Datapath 20 points. Canvas Q42-Q51
  - 42. What is encoding that supports `RELU` ?
  - 43. Which instruction field can be written to memory in the baseline pipeline?
  - 44. Consider the following modifications to the source `Reg[]` inputs. Which configuration will allow this instruction to execute correctly without breaking the ex-ecution of other instructions in our instruction set?
  - 45. Consider the following modifications to the `Branch` . Which con-figuration will allow this instruction to execute correctly without breaking the ex-ecution of other instructions in our instruction set? Branch calculates `A==B` and `A<B`
  - 46. Consider the following modifications to the `DMEM` inputs. Which is correct?
  - 47. Consider the following modifications to the `DMEM` control signal. Which is correct ?
  - 48. Consider the following modifications to the `WB` . Which configuration will allow this instruction to execute correctly
  - 49. Consider the following modifications to the `RegWEn` mux inputs. Which configuration will allow this instruction to execute correctly
  - 50. What is the value of ASel?
  - 51. What is the value of BSel?
- F. RISC-V Program 10 points. Canvas Q52-Q53
  - 52. What 8 memory locations are modified. 5 points
  - 53. What is the value in those memory locations. 5 points

Section Virtual Memory 22 points. Canvas Q1-Q22

The chart below shows how memory accesses are treated in a system. The table below describes the parameters int he memory system. Please use the data below to answer question groups Q1,Q2,Q3,Q4 on canvas.

```
CAUTION: When converting from binary to hex you can always pad the MSB
e.g., 10 1010 (6 bit field) in hex is 0010 1010 (2 0s padded in MSB)
is 0x2a .
```



Parameter	Value
Physical address bits	18
Size of page	1KB or 1024 bytes
Virtual address bits	22
----------	----------
TLB Sets	4
TLB Ways	4
TLB Size	16 entries
----------	----------
Cache block	16 bytes
Cache size	256 bytes
Cache Sets	4
Cache Ways	4

Terminology

- VPN - Virtual page number
- Index (Set index of cache or TLB)
- PPN - Physical page number
- INVALID. TLB entry is invalid
- TLB-T (TLB Tag)

TLB State

Way 0	PPN
TLB-T:[0xe8] Index:[0x0]	INVALID
TLB-T:[0x2fa] Index:[0x1]	0x8d
TLB-T:[0x71] Index:[0x2]	INVALID
TLB-T:[0x2ca] Index:[0x3]	0x70

Way 1	PPN
TLB-T:[0x23c] Index:[0x0]	0x91
TLB-T:[0x2fc] Index:[0x1]	0xfa
TLB-T:[0x5] Index:[0x2]	0x99
TLB-T:[0x2db] Index:[0x3]	0x13

Way 2	PPN
TLB-T:[0x1ce] Index:[0x0]	INVALID
TLB-T:[0x301] Index:[0x1]	0xbd
TLB-T:[0x236] Index:[0x2]	INVALID
TLB-T:[0x21a] Index:[0x3]	INVALID

Way 3	PPN
TLB-T:[0x118] Index:[0x0]	INVALID
TLB-T:[0xf] Index:[0x1]	0x33
TLB-T:[0x298] Index:[0x2]	INVALID
TLB-T:[0x29d] Index:[0x3]	0x1f

Page Table (Partial)

```
CAUTION: Only partial table relevant to the questions are shown.
```

VPN	PPN	Valid
0xb2b	0x70	1
0x8e9	0x8d	1
0xc05	0xba	1
0x2db	0x13	1
0x738	----	0
0x3a0	----	0
0xbe9	0x9d	1
0x1c6	----	0
0x8f0	0x91	1
0xbf1	0x47	1
0x016	0x99	1

Cache State

- Way 0

Way 0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Tag: [0x917] Set:0	0xe8	0x13	0x9e	0x26	0xaf	0xc5	0x72	0x44	0xbc	0x6d	0x78	0x50	0x66	0x2f	0x66	0x8f
Tag: [0x8d5] Set:1	0xe4	0x2b	0x0d	0xd3	0xa0	0xb2	0x0f	0x9a	0xe9	0x7e	0xc8	0x0e	0x1e	0x13	0xea	0x6a
Tag: [0x707] Set:2	0x5a	0xd9	0xc9	0x38	0x50	0xba	0x35	0x0c	0x4c	0x8c	0xd7	0xc7	0xaa	0x79	0x2f	0x0d
Tag: [0x7b7] Set:3	0x57	0xb4	0x4c	0xda	0x4a	0xbb	0xc6	0x25	0x8c	0x5f	0x7a	0x24	0xd5	0xac	0xc4	0xc3

- Way 1

Way 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Tag: [0x133] Set:0	0x4f	0xa0	0x34	0x03	0x7c	0x72	0x20	0x46	0x12	0xbd	0x7b	0x74	0xbe	0xf7	0x38	0x11
Tag: [0x761] Set:1	0xb9	0x0f	0x68	0x06	0xe4	0xb7	0xad	0x7d	0xca	0xb1	0x83	0x10	0xa2	0x9e	0x9f	0xd8
Tag: [0x336] Set:2	0x27	0x90	0x08	0x04	0x50	0xbe	0xd8	0x7b	0x92	0x08	0x9b	0xb7	0x6d	0xe1	0xc2	0x2e
Tag: [0xbaf] Set:3	0xcb	0x7d	0x7e	0x48	0x04	0x40	0xba	0x33	0x79	0xca	0x50	0x1d	0x4f	0xf5	0xbd	0x8e

- Way 2

Way 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Tag: [0x39] Set:0	0xe6	0x03	0x8b	0x4f	0xcc	0x42	0x16	0xa7	0xd0	0x8d	0x9b	0x7d	0x9e	0x10	0x36	0x9d
Tag: [0xdc0] Set:1	0x47	0x8f	0x7a	0x8f	0x70	0x57	0xbd	0x90	0xef	0xec	0x5f	0xb4	0x1e	0x62	0xe8	0xd6
Tag: [0x1f8] Set:2	0xce	0xbd	0xa3	0xd5	0x22	0x46	0xb9	0x27	0xee	0x57	0x28	0xe8	0x7a	0x27	0x2f	0x3c
Tag: [0xfab] Set:3	0xee	0xef	0xe6	0xcd	0x00	0xe7	0x3f	0xd9	0x65	0xd0	0xcc	0x60	0x27	0x80	0x7b	0xe3

- Way 3

Way 3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Tag: [0x2b0] Set:0	0x35	0x76	0x31	0xa3	0x23	0x54	0x74	0x1e	0xc1	0x16	0xd3	0x18	0x59	0xfb	0xdf	0x2a
Tag: [0xbdd] Set:1	0xc5	0x87	0x52	0x27	0x94	0xcd	0xe4	0x53	0xeb	0xb5	0xa2	0xd9	0x28	0x61	0x34	0x43
Tag: [0x47c] Set:2	0xbe	0xd0	0xfa	0xd1	0xad	0x91	0xb4	0xb4	0x2c	0x43	0xce	0x45	0xc0	0xdb	0x73	0x44
Tag: [0x815] Set:3	0x27	0x3f	0xce	0xd8	0xc7	0x1d	0xbe	0x2c	0xa5	0x4f	0x0d	0x13	0x55	0xde	0xa5	0xed

Common questions. Canvas Q1-Q2

1. How many bits is the VPN ?

2. How many bits is the PPN ?

For the virtual address 0x2cade0 answer the following Canvas Q3-Q12

- What is the VPN
- What is the TLB tag.
- Is it a TLB hit or miss
- Is it a page fault
- What is the PPN ?
- what is the cache tag ?
- what is the cache index
- What is the byte offset
- Is it a cache hit or miss
- What is the data byte

For the virtual address 0x301754 answer the following. Canvas Q13-Q22

- What is the VPN
- What is the TLB tag.
- Is it a TLB hit or miss
- Is it a page fault
- What is the PPN ?
- what is the cache tag ?
- what is the cache index
- What is the byte offset
- Is it a cache hit or miss
- What is the data byte

B. Section Cache I Questions. 15 points. Canvas Q23-Q25

Let the A[0] be at 0x00000 and B[0] be at 0x100### 00. The size of an integer is 4 bytes. Size of each array is 1024 ints. Describe the behavior of the following code when run on the cache and answer the questions. Assume that there is 1 level of cache and it is completely empty when starting this program. The size of the cache is 2 KB, 16 sets, 16 ways and 8 byte blocks.

```
int A[1024], B[1024];
void loops() {
  // Loop 1
  for (int index = 0; index < 32; index++) {
    B[index] = 0xff;
    A[index] = 0xff;
  }
  // Loop 2
  for (int index = 32; index < 1024 index++) {
    B[index] = B[index - 16] + A[index -  16] ;
    A[index] = B[index -  8] + A[index -  8] ;
  }
}
1 level of cache
+--------------+
|  16 sets     |
|  16 ways     |
|  8 byte block|
+--------------+

```

23. What is the miss rate for loop 1? (Assume that only loop 1 runs). 5 points

24. What is in the cache at the end of loop 1? 5 points

25. What is the miss rate for loop 2 ? Assume that loop 1 has already run to completion and has warmed up the cache. 5 points

C. Section Cache II Questions. 20 points. Canvas Q26-Q31

```
int src[2048]; Address - 0x0000
int dest[2048]; Address - 0x1000
for (int i = 0; i<2048; i += 4) {
  b[i] = a[i];
}

Cache Parameters

sizeof(int) - 4 bytes
1 level of cache
+------------------------+
|  512 byte              |
|Direct mapped           |
|32 bytes/block or 8 ints|
+------------------------+

Cache layout

    1 way (Direct mapped)
    +------------------+
    |(32 byte or 8 int)|
    +------------------+
    |                  |
    +------------------+
16  |                  |
sets+------------------+
```

26. Assuming the total size of the physical address is 32 bits. What is the number of bits required by tag, index and offset (4 points)

27. What is the hit rate of this direct-mapped cache? (4 points)

28. What type of misses occur (Conflict, Compulsory, Capacity) ? (2 points)

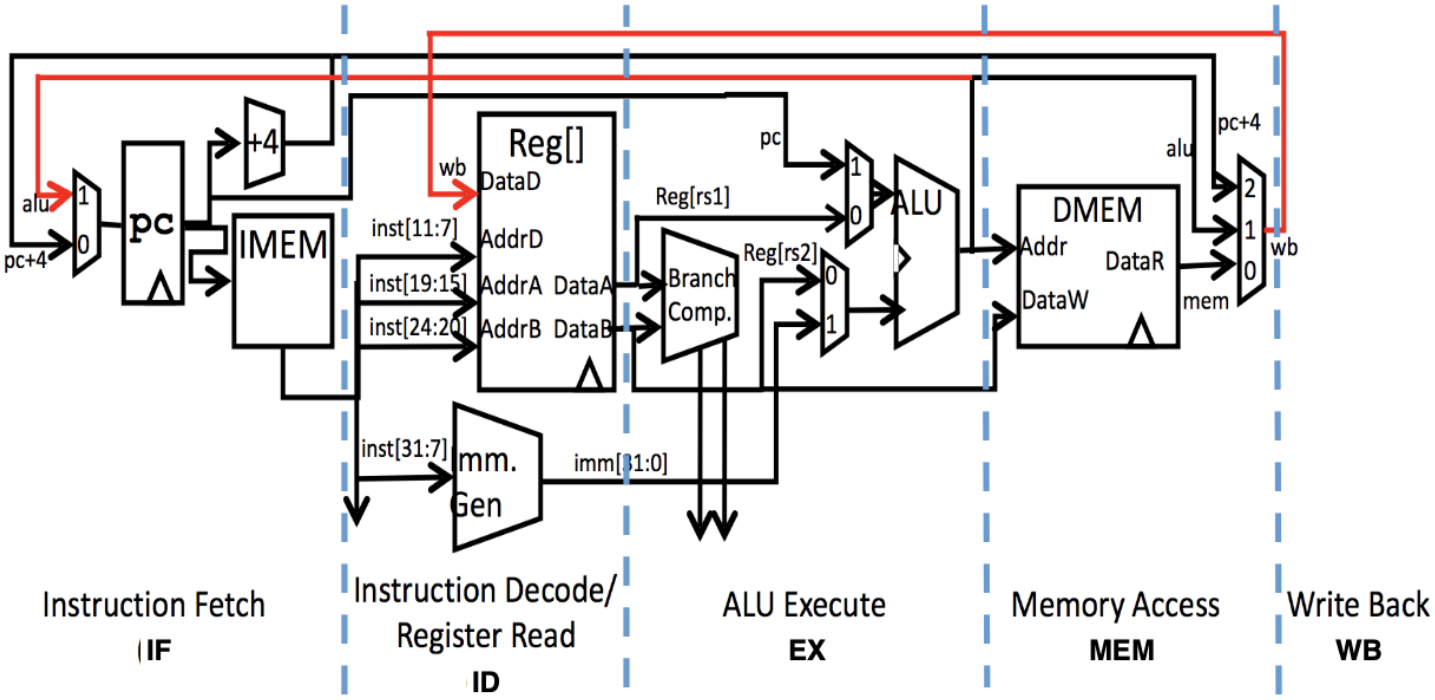
29. What is the hit rate a 2-way set associative cache. 512 bytes. 8 words/block. (4 points)

30. What type of misses occur (Conflict, Compulsory, Capacity) in the 2-way cache ? (2 points)

31. Now consider a 4-way set associative cache. 512 bytes. 8 words/block.What is the hit rate ? (4 points)

D. RISC-V Pipeline 20 points. Canvas Q32-Q41

Consider a typical 5-stage (Fetch,Decode,EXecute,Memory,WriteBack) pipeline.Assume pipeline registers exist where the dotted lines are



This pipeline is more simple than the one you dealt with in the assignment.

- Forwarding/Bypassing is not implemented; dependent instructions have to wait.
- Following a branch, the next instructions always fetches from PC+4 until the branch is resolved in the WB stage (`CAUTION: Note that the lecture slides resolved branch in the EX stage`). Flush the pipeline if branch is taken.
- We can read and write from the same registers or memory location in the same clock cycle. Any memory location can be accessed.

Answer questions based on the following program

```
1  addi x9, x0, 0xF    # Instruction 1
2  addi x18, x0, 0     # Instruction 2
3  beq x9, x18, exit   # Instruction 3
4  lw x9, 10(x8)       # Instruction 4
5  xor x9, x9, x18     # Instruction 5
6  exit:
7    sw x9, 10(x8)     # Instruction 6
```

`Hint: Start by creating a pipeline sheet similar to Assignment 6 (with pen and paper)`

32. In which cycle does `addi x18,x0,0` (instruction 2) run the EX stage ?

33. In which cycle does `beq x9,x18,exit` (instruction 3) read the registers?

34. In which cycle does the `lw x9, 10(x8)` (instruction 4) start the IF stage ?

35. In which cycle does the `lw x9, 10(x8)` read the registers ?

36. In which cycle does the `xor x9, x9, x18` (instruction 5) reach the IF stage ?

37. In which cycle does the `xor x9,x9,x18` (instruction 5) read the registers ?

38. In which stage is `sw x9, 10(x8)` stalled and how many cycles?

39. In which cycle does the `sw x9, 10(x8)` (instruction 6) write the memory location ?

40. How many instructions are stalled due to data hazards ?

41. How many cycles do we have stall in total for this program ? i.e., Consider a program with 6 instruction and no hazards and ran to completion in T cycles. This program completed in T_hazard cycles. What is (T_hazard - T)?

E. RISC-V Datapath 20 points. Canvas Q42-Q51

We wish to introduce a new instruction into our RISC-V datapath.
`RELU` . This is related to the relu operation in assignment 3. We are going to be replacing a multiple instruction sequence with a single RELU instruction works as follows.

```
1  # rd_rs2, is a register that acts as a source
2  # and destination register
3  RELU rd_rs2, offset(rs1)
4
5  ***Operation description of RELU***
6  if (0<=R[rd_rs2])
7    MEM[R[rs1]+offset] = R[rd_rs2]
8  else
9    MEM[RS[rs1]+offset] = 0
10   R[rd_rs2] = 0
```

It combines the semantics of branch, load and store.

- Like a store it performs arithmetic using the ALU for calculating `R[rs1]+offset` the memory address to be modified.
- Like a store it updates the MEM[address] with a value. But the value depends on branch outcome.
- Like a branch it performs comparison. However the operands used are different.
- Typically, the branch comparison will modify PC. However, here the branch comparison influences what value is stored to Memory, either R[rd_rs2] or 0.
- - Like a load it updates the register value, but depends on the branch outcome. The branch comparison influences the value of rd in a load operation, if the branch comparison fails the R[rd_rs2] is 0, otherwise rd_rs2 is not updated.

```
Caution 1: In a typical RISC-V instruction rs2 field is used as source only and rd as destination only.
In this case we are using the rd field also as a source when performing the comparison operation line 4
and writing to memory (line 5). We are also using rd field as a destination register in line 8.
```

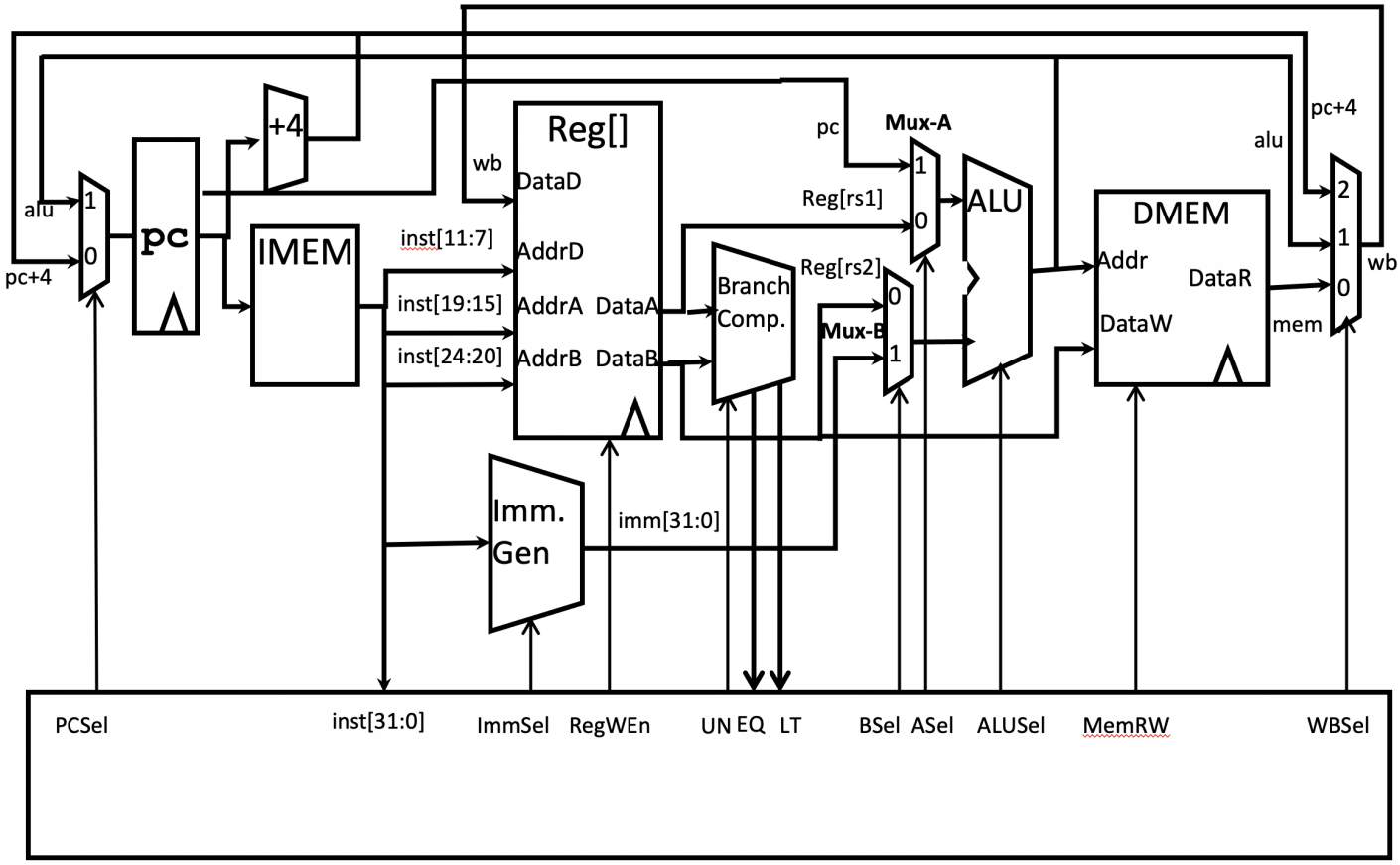
Given the single cycle datapath below, select the correct modifications in parts such that the datapath executes correctly for this new instruction (and all other instructions!). You can make the following assumptions:

- We have a new control signal `RELU` which is 1 if the instruction being decoded is a RELU
- ALUsel is add when we have a RELU instruction
- The immediate generate sign extends the offset similar to load instructions.

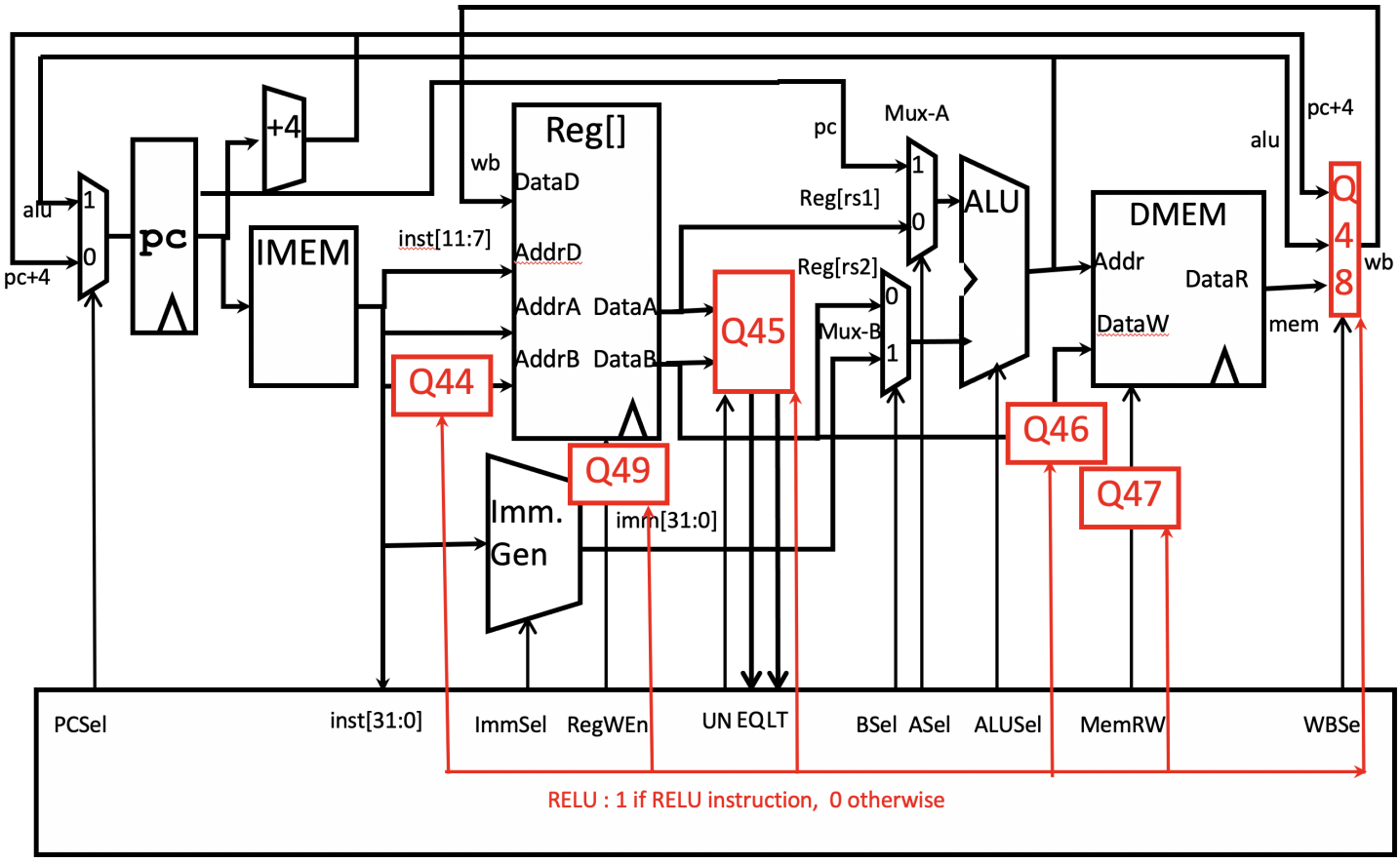
```
Caution 2: Pay careful attention to which input line is 1 and which line is 0 in the muxes.
Some muxes choose top-most input as 0, some choose bottom-most input as 0
```

```
Hint: YOU DO NOT REQUIRE TRUTH TABLES
Try writing down in plain english or reading out the logic
to yourself e.g, !(A<=B) is A is not equal to B and A is not LT (less than) B
```

Baseline Pipeline



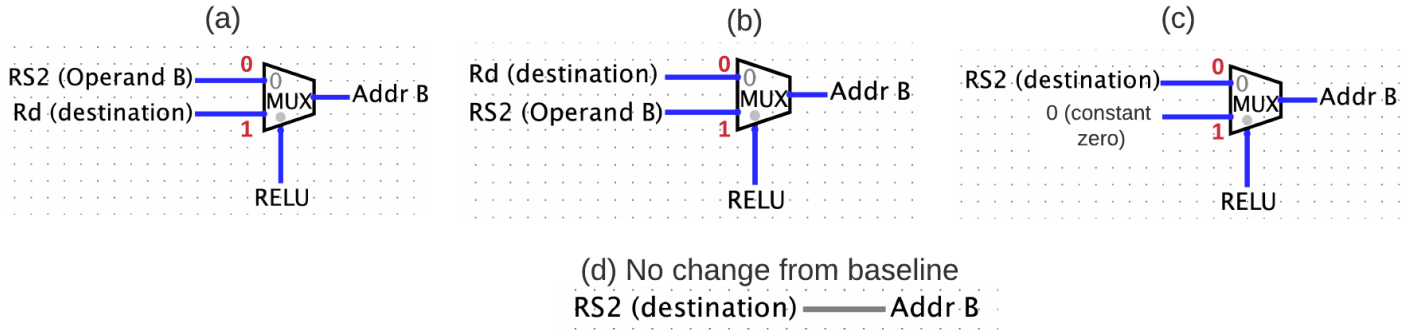
Pipeline with RELU (Red boxes indicate questions)



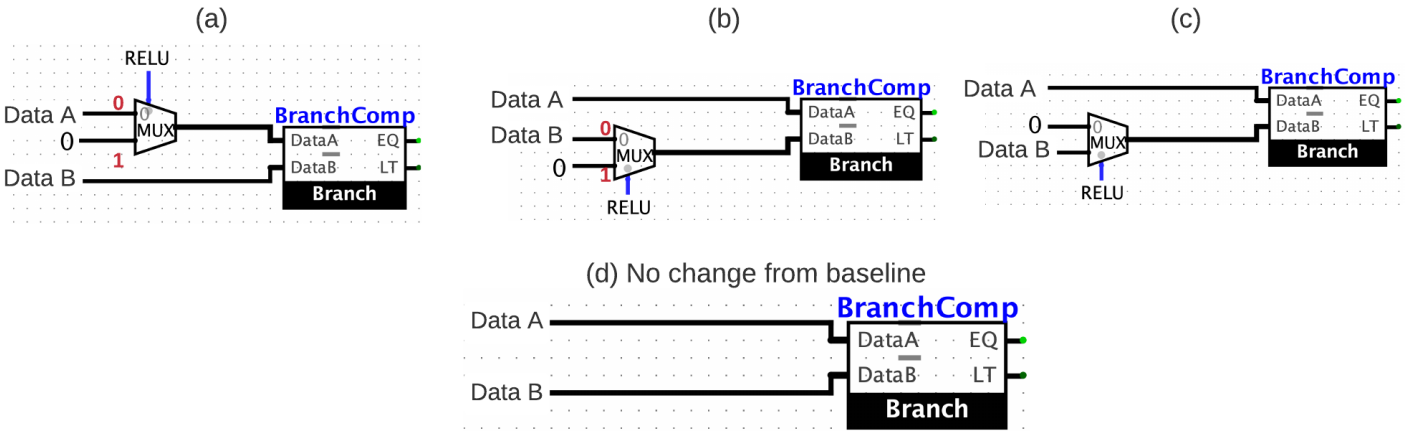
42. What is encoding that supports `RELU` ?

43. Which instruction field can be written to memory in the baseline pipeline?

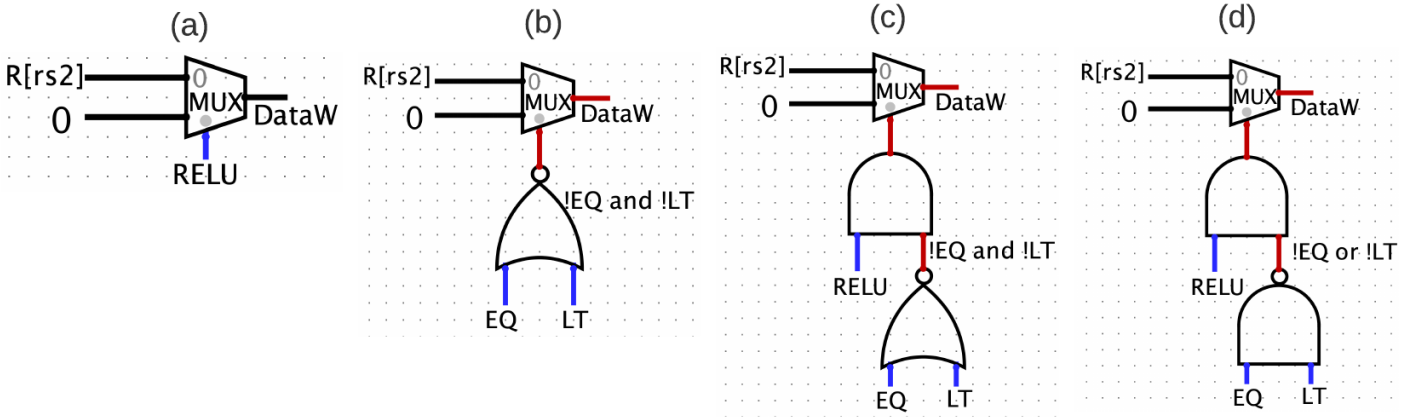
44. Consider the following modifications to the source `Reg[]` inputs. Which configuration will allow this instruction to execute correctly without breaking the ex-ecution of other instructions in our instruction set?



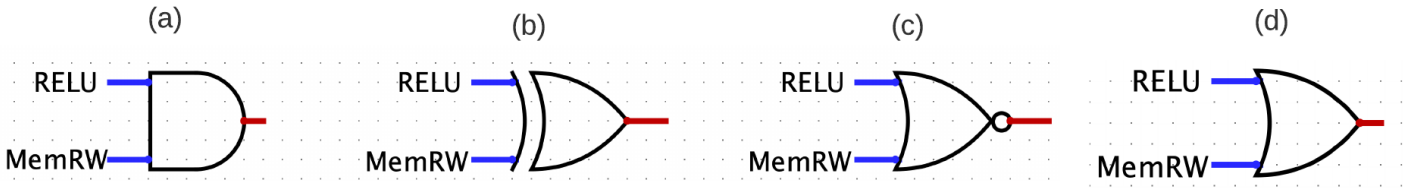
45. Consider the following modifications to the `Branch` . Which con-figuration will allow this instruction to execute correctly without breaking the ex-ecution of other instructions in our instruction set? Branch calculates `A==B` and `A<B`



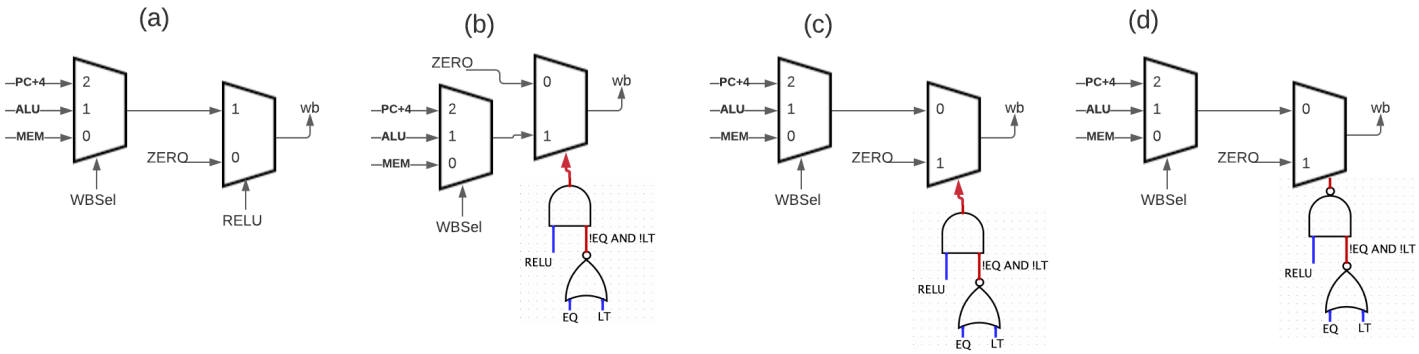
46. Consider the following modifications to the `DMEM` inputs. Which is correct?



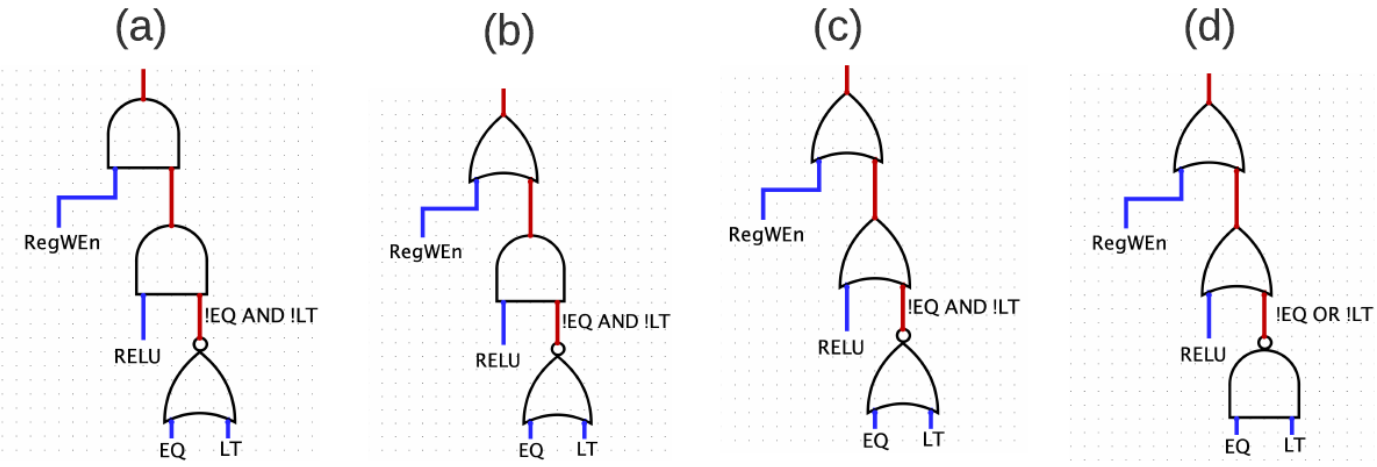
47. Consider the following modifications to the `DMEM` control signal. Which is correct ?



48. Consider the following modifications to the `WB` . Which configuration will allow this instruction to execute correctly



49. Consider the following modifications to the `RegWEn` mux inputs. Which configuration will allow this instruction to execute correctly



50. What is the value of ASel?

51. What is the value of BSel?

F. RISC-V Program 10 points. Canvas Q52-Q53

We will be introducing a new instruction called `lwa` in RISC-V. In baseline RISCV the loads calculate addresses using an immediate and register. However, in many programs typically the address is calculated using 2 registers. The semantics of the `lwa` instruction (lwa rd,rs1,rs2) are dst = MEM[rs1+rs2] e.g., lets say a0=0x4 a1=0x1000 lwa a2,a1,### a0. a2 = MEM[0x1004]

You want to impress your friend, so you predict the result of executing the program as it is written, just by looking at it. If the program is guaranteed to execute without crashing, describe what it prints, otherwise explain the bug that may cause a crash.

```
.globl main
.data
a: .string "skayaks"
table: .string "ZYXWVUTSRQPONMLKJIHGFEDCBA12345"
init: .string "XXXXXXX" # 7 Xs

.text
cipher:
     addi    s3,zero,25

loop_header:
        lbu  s2, 0(a0) # Read character ch
        beqz s2, end
        addi s7,a0,0
  addi a0,a0,1
        la s4,table
loop:
   addi s1, s2, -97 #
   bltu s3,s1,loop_header
         andi s2,s2,0x1F
   lwa  s2,s2,s4 # New instruction
   sb   s2, 0(a1)
   addi a1,a1,1
   j loop_header
end:
         ret

main:
   la a0, a
   la a1,init
   jal cipher   li a0,10
   ecall
```

52. What 8 memory locations are modified. 5 points

53. What is the value in those memory locations. 5 points