HONOR CODE

- I have not used any online resources during the exam.
- I have not obtained any help either from anyone in the class or outside when completing this exam.
- No sharing of notes/slides/textbook between students.
- NO SMARTPHONES.
- **CANVAS ANSWERS MAY BE LOCKED AFTER 1ST TRY.**

Questions Sheet.

Read all of the following information before starting the exam:

- For each question fill out the appropriate choice and write text on Canvas page. Also type clearly on in the exam on the appropriate text.
- For essay questions (non multiple choice). Write down the answer first and then 1/2 sentences with reasons.
- IF THE MULTIPLE CHOICE ANSWER IS WRONG WE WILL MARK THE ANSWER WRONG. IF THE MULTIPLE-CHOICE ANSWER IS CORRECT, WE WILL READ THE WRITTEN PORTION.
- Show all work, clearly and in order, if you want to get full credit.
- I reserve the right to take off points if I cannot see how you logically got to the answer (even if your final answeris correct).
- Circle or otherwise indicate your final answers.
- Please keep your written answers brief; be clear and to the point.
- I will take points off for rambling and for incorrect or irrelevant statements. This test has seven problem sets.
- You have to upload your worksheet/scrap to coursys after you complete the exam. You have up to 11:59pm Aug 14th to do that.

- HONOR CODE
- Questions Sheet.
- Section Virtual Memory 17 points. Canvas Q1-Q31
  - Common questions. Canvas Q1-Q2
  - For the virtual address 0x11a39 answer the following Canvas Q3-Q12. All in hex. (0.5 pt each)
  - For the virtual address 0xab6e7 answer the following. Canvas Q13-Q22. All in hex (0.5 pt each)
  - c. For the following virtual address 0x02974 answer the following. All in hex (Canvas: 23-32) (0.5 pt each)
- B. Easy. RISCV Blackbox. [10 Points]
  - 33. What is the value of the registers a0,a1, a2 on line 5: CHECK ? (show your working and explain your answer). Write down in hex [5]
  - 34. Lets say message* is now a 2 character string "J-". The value of a2 on line 5:CHECK is 0. What is the mystery character "-". It has to be an ascii character between '0'--'9' (note not value 0-9). ? Write down the digit. [5]
- C. Lets Cache I (10pts)
  - 35. What is the number of tag bits in Cache-A and Cache-B ? (1pt)
  - 36. What is the number of index bits in Cache-A and Cache-B ? (1pt)
  - 37. What is the number of offset bits in Cache-A and Cache-B ? (1pt)
  - 38. What is the hit rate for Cache-A and Cache-B for loop 1? What types of misses do we get? (2 pts)
  - 39. What is the hit rate for Cache-A and Cache-B when you execute loop 2? (5 pts)
- D. Lets Cache II (10pts)
  - 40. What is the bits for virtual address? (1)
  - 41. What is the bits for physical address? (1)
  - 42. Which associativity below will maximize cache size while maintaining the same Tag:Index:Offset? (1)
  - 43. Which block size below will maximize cache size while maintaining the same Tag:Index:Offset? (1)
  - 44. Assuming associativity and block size from questions 42 and 43 what is the number of blocks? (1)
  - 45. Now we're working with a direct mapped cache with same TIO and block size as 43. What is miss rate for code below (3)
  - 46. You add an L2 and shrink the L1. L1 hit latency is 3 cycles. L2 hit latency is 50 cycles. L2 hit rate is 90%. L1 hit rate is 25%. Memory is 100 cycles What is AMAT ? (2)
- E. RISC-V Single Cycle Datapath 16 points.
  - 47. What is the number of register that beqjalr needs to read and write in a single cycle ? (1)
  - 48. What is the RegWEn signal ? (1)
  - 49. What is the branch comparison signal we are interested in? (1)
  - 50. Which fields are passed to the branch comparison ? (1)
  - 51. What is the logic for beqjalr signal ? (1)

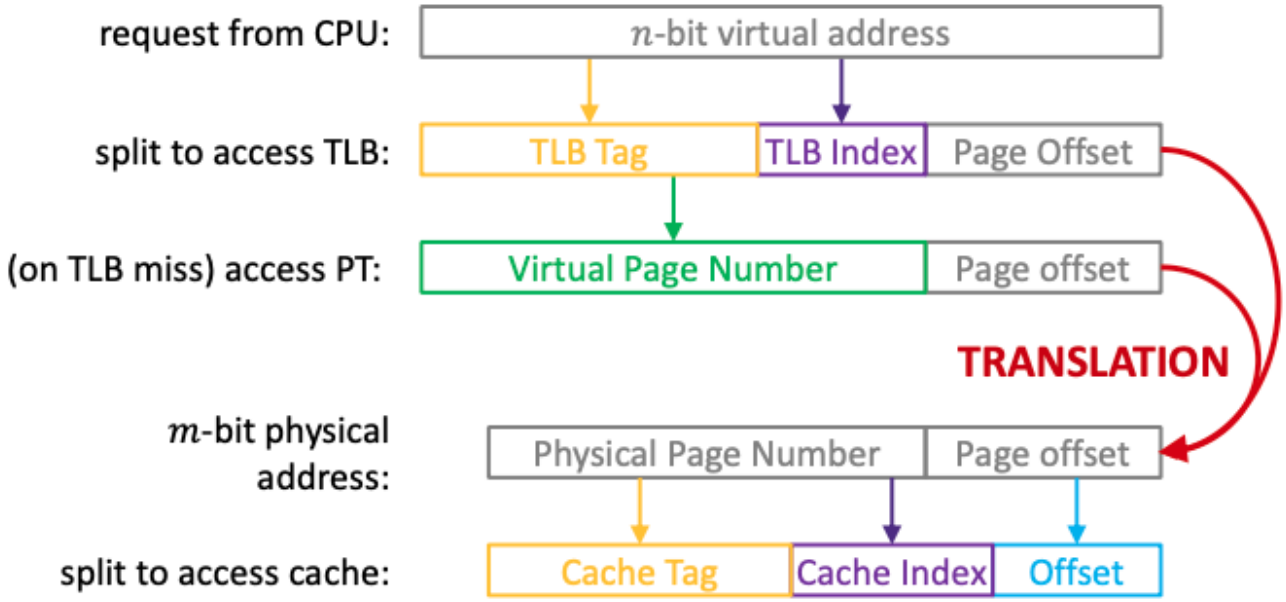
    - 52. Consider the following modifications to the Reg[] register file. (2)
    - 53. What are the inputs to the register file ? (2)
    - 54. What are the inputs to the ALU ? (1)
    - 55. What are the changes to mux-A ? (2)
    - 56. What are the changes to mux-B ? (2)
    - 57. For beqjalr instruction which signal does WBsel choose ? (2)
    - 58. What are the changes to the writeback stage ? (2)
- F. RISC-V Pipeline 12 points.
    - 59. What hazards existing between instruction 1 and 2 ? (1)
    - 60. What hazards existing between instruction 2 and 3 ? (1)
    - 61. What hazards existing between instruction 3 and 4 ? (1)
    - 62. What hazards existing between instruction 4 and 5 ? (1)
    - 63. How many cycles does instruction 2 stall for ? (2)
    - 64. How many cycles does instruction 3 stall for ? (2)
    - 65. How many cycles does instruction 4 stall for ? (2)
    - 66. How many cycles does instruction 5 stall for ? (2)
- G. Lets RISC-V II 10 points
    - 67. We are designing a new RISC-V instruction with 16 registers. Assuming that you use the extra bits to extend the immediate field, what is the range of `half-word` instructions that can be reached using a branch instruction in this new format? (2)
- Refer code below for remaining questions
    - 68. What is the PC address of `instruction 4:beq` (hex) ?
    - 69. What is the PC address of `instruction 9:addi` (hex) ?
    - 70. What is the PC address of `instruction 12:ecall` (hex) ?
    - 71. What is the PC address of `instruction 14:mul` (hex) ?
    - 72. What is the machine code for instruction at address 0x1C (hex) ? (2)
    - 73. After the first pass of the assembler instruction at 0d20 does not have the label resolved. (1)
    - 74. After the first pass of the assembler instruction at 0d28 does not have the label resolved. (1)

Section Virtual Memory 17 points. Canvas Q1-Q31

```
Refer slide deck L21-VM-III Week 8 if you need to.
```

The chart below shows how memory accesses are treated in a system. The table below describes the parameters int he memory system.
Please use the data below to answer question groups Q1,Q2,Q3,Q4 on canvas.

```
CAUTION: When converting from binary to hex you can always pad the MSB
e.g., 10 1010 (6 bit field) in hex is 0010 1010 (2 0s padded in MSB)
is 0x2a .
```



Parameter	Value
Physical address bits	16
Size of page	256 bytes
Virtual address bits	20
----------	----------
TLB Sets	4
TLB Ways	2
TLB Size	8 entries
----------	----------

Parameter	Value
Cache block	8 bytes
Cache size	64 bytes
Cache Sets	8
Cache Ways	1

- VPN - Virtual page number
- Index (Set index of cache or TLB)
- PPN - Physical page number
- INVALID. TLB entry is invalid
- TLB-T (TLB Tag)

TLB

Way 0	PPN
Index:0 TLB-T:[0x69]	---
Index:1 TLB-T:[0x396]	---
Index:2 TLB-T:[0x46]	eb
Index:3 TLB-T:[0x29c]	4a

Way 1	0
Index:0 TLB-T:[0x3b]	---
Index:1 TLB-T:[0x010]	88
Index:2 TLB-T:[0x2ad]	4b
Index:3 TLB-T:[0x6]	dc

Page Table (Partial)

```
CAUTION: Only partial table relevant to the questions are shown.
```

VPN	PPN	Valid
0x1a4	---	0
0xe59	---	0
0x11a	0xeb	1
0xa73	0x4a	1
0xec	0x00	1
0x29	0x12	1
0xab6	0x4b	1
0x1b	0xdc	1
0x8ff	0x91	1
0xbf1	0x47	1
0x016	0x99	1
0x010	0x88	1

Cache

- Way 0

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Index: 0 Tag: [0x3ae]	0x39	0x24	0x76	0x62	0x17	0x92	0x72	0x38
Index: 1 Tag: [0x373]	0x24	0x6c	0x38	0x47	0x8e	0x43	0xc2	0x29
Index: 2 Tag: [0x2c7]	0x08	0x9d	0xd1	0xf8	0x53	0x05	0x14	0x16
Index: 3 Tag: [0xdc]	0xfa	0x8c	0x3d	0x11	0x14	0xf4	0xe9	0xc3
Index: 4 Tag: [0x12b]	0x11	0xfa	0x4c	0x9d	0xb3	0x1d	0xb6	0x87
Index: 5 Tag: [0x27e]	0xdc	0x0f	0x44	0x85	0x6b	0xfc	0x04	0x4f
Index: 6 Tag: [0x49]	0x38	0xde	0xfb	0x10	0x3d	0xfe	0x05	0xc5
Index: 7 Tag: [0x3ac]	0x49	0x52	0xe0	0xdd	0xf0	0x0d	0xa6	0xe0

Common questions. Canvas Q1-Q2

1. How many bits is the VPN. decimal (1pt) ?
2. How many bits is the PPN. decimal (1pt) ?

For the virtual address 0x11a39 answer the following Canvas Q3-Q12. All in hex. (0.5 pt each)

- What is the VPN
- What is the TLB tag.
- Is it a TLB hit or miss
- Is it a page fault
- What is the PPN ?
- what is the cache tag ?
- what is the cache index
- What is the byte offset
- Is it a cache hit or miss
- What is the data byte

For the virtual address 0xab6e7 answer the following. Canvas Q13-Q22. All in hex (0.5 pt each)

- What is the VPN
- What is the TLB tag.
- Is it a TLB hit or miss
- Is it a page fault
- What is the PPN ?
- what is the cache tag ?
- what is the cache index
- What is the byte offset
- Is it a cache hit or miss
- What is the data byte

c. For the following virtual address 0x02974 answer the following. All in hex (Canvas: 23-32) (0.5 pt each)

- What is the VPN
- What is the TLB tag.
- Is it a TLB hit or miss
- Is it a page fault

- What is the PPN ?
- what is the cache tag ?
- what is the cache index
- What is the byte offset
- Is it a cache hit or miss
- What is the data byte

B. Easy. RISCV Blackbox. [10 Points]

WARNING: FOR THIS QUESTION MAKE SURE YOU WRITE YOUR CORRECT ANSWER AT THE BEGINNING. ALSO WRITE ONE/TWO SENTENCES REASONING YOUR ANSWER. OTHERWISE WE WILL SIMPLY ZERO IT OUT.

Assume we have two arrays input and output.

```
char *message = "MESSAGE"
```

Study the following RISC-V code shown below and answer the questions. You can assume the data segments starts at 0x10000000 and only contains message. You can assume a0 contains value of message* at the start.

```
.text
main:
  li  a2,0xFF
  jal BLACKBOX
  # CHECK
  li a0,10
  ecall

BLACKBOX:
  addi sp,sp,-4
  sw ra, 0(sp)

  lbu  a1,0(a0)
  beq a1,zero,end
  and a2,a1,a2
  addi a0,a0,1
  jal BLACKBOX

end:
  lw ra, 0 (sp)
  addi sp,sp,4
  ret
```

33. What is the value of the registers a0,a1, a2 on line 5: CHECK ? (show your working and explain your answer). Write down in hex [5]

34. Lets say message* is now a 2 character string "J-". The value of a2 on line 5:CHECK is 0. What is the mystery character "-". It has to be an ascii character between '0'--'9' (note not value 0-9). ? Write down the digit. [5]

C. Lets Cache I (10pts)

Assume we are working in a 4GB physical address space.

Cache-A	Direct-mapped, 4KB, 512 byte blocks
Cache-B	Set-associate, 4KB, 2 ways, 512 byte block

Both caches use write-back and write-allocate policies.
Answer questions below

```
int size = 2 * 1024;
// long long int is 8 bytes
long long int array[size];
/* loop 1 */
for (int i = 0; i < size; i++) {
  array[i] = i;
}

/* loop 2 */
for (int i = 0; i < size; i += 8) {
// Order in which access happens
//3rd       1st        2nd
array[i] =  array[i] * arr[0];
}
```

35. What is the number of tag bits in Cache-A and Cache-B ? (1pt)

36. What is the number of index bits in Cache-A and Cache-B ? (1pt)

37. What is the number of offset bits in Cache-A and Cache-B ? (1pt)

38. What is the hit rate for Cache-A and Cache-B for loop 1? What types of misses do we get? (2 pts)

39. What is the hit rate for Cache-A and Cache-B when you execute loop 2? (5 pts)

D. Lets Cache II (10pts)

We have a mystery cache. A mystery, byte addressed cache has Tag:Index:Offset (T:I:O) = 12:4:3.

40. What is the bits for virtual address? (1)

41. What is the bits for physical address? (1)

42. Which associativity below will maximize cache size while maintaining the same Tag:Index:Offset? (1)

43. Which block size below will maximize cache size while maintaining the same Tag:Index:Offset? (1)

44. Assuming associativity and block size from questions 42 and 43 what is the number of blocks? (1)

45. Now we're working with a direct mapped cache with same TIO and block size as 43. What is miss rate for code below (3)

```
#define LEN 2048
int ARRAY[LEN];
int main() {
    for (int i = 0; i < LEN - 32; i+=32) {
       ARRAY[i] = ARRAY[i] + ARRAY[i+1] + ARRAY[i+32];
       ARRAY[i] += 10;
}
```

46. You add an L2 and shrink the L1. L1 hit latency is 3 cycles. L2 hit latency is 50 cycles. L2 hit rate is 90%. L1 hit rate is 25%. Memory is 100 cycles What is AMAT ? (2)

E. RISC-V Single Cycle Datapath 16 points.

We wish to introduce a new instruction into our RISC-V datapath.
`beqjalr` . This instruction is a conditional jal instruction. Typical branch instruction has limited offsets since all offsets are PC-relative. Jalr however can specify register relative. The instruction works as follows. The instruction is encoded as follows.

- We no longer use an immediate for the branch offsets
- We revert imm[4:1|11] to specify a register

`original beq instruction`

imm[12	10:5]	rs2	rs1	0x0	imm[4:1

`new beqjalr instruction`

f7 (0x40)	rs2	rs1	0x0	rd	1100011

```
if (R[rs1] == R[rs2]) {
 R[ra] = PC + 4;
 PC = R[rd];
} else  {
// Zero out the rd register and destroy
 R[rd] = 0
}

```

It combines the semantics of branch, JALR and R-type instruction.

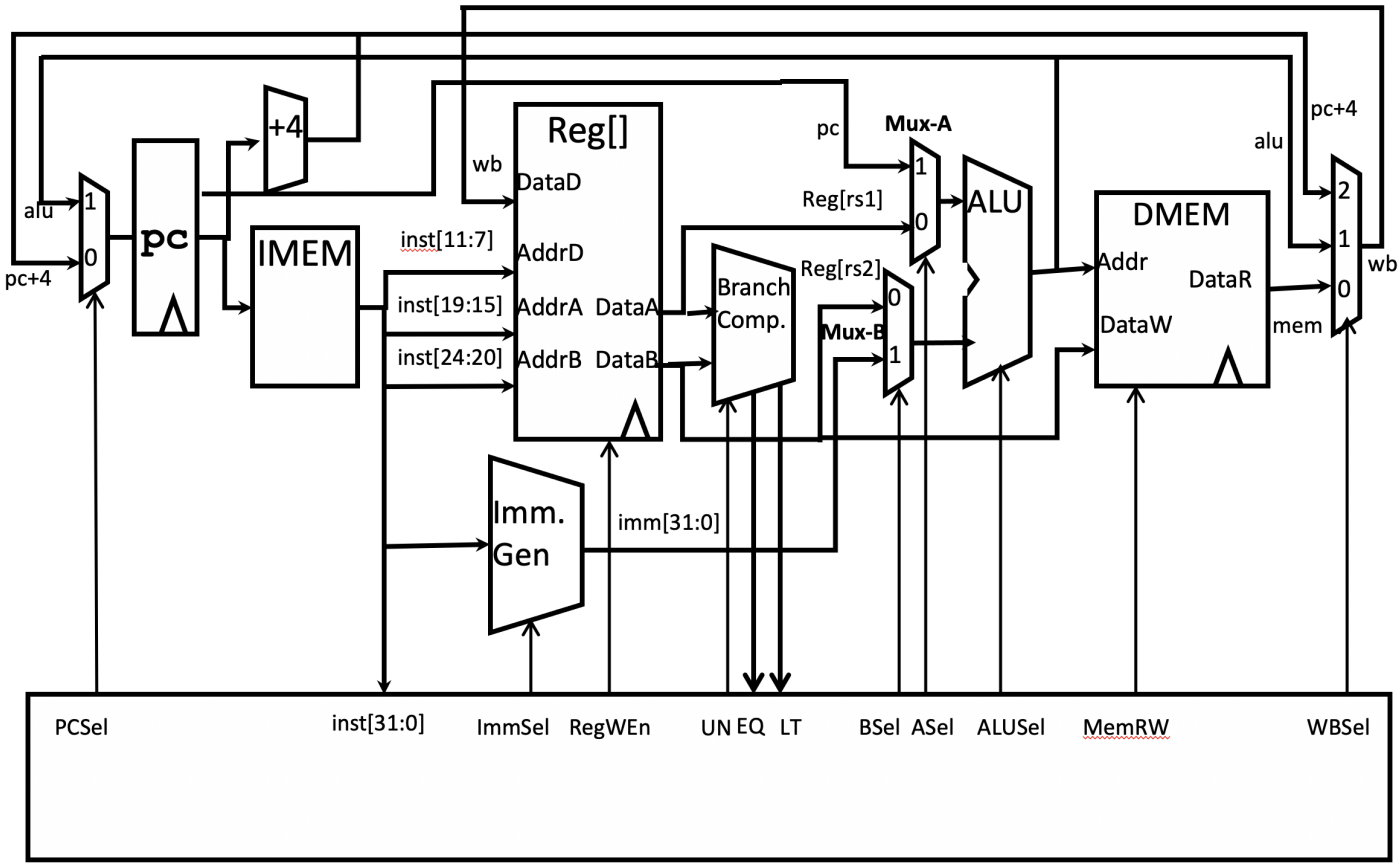
- Like a branch it performs a comparison.
- If comparison succeeds it performs a JALR, the destination is contained in the rd register.
  `rd is treated as a source` .
- If comparison fails, it simply zeros out the register which contains the PC it should jump to.
  `rd is treated as a destination`
- We have a new control signal `beqjalr` which is 1 if the instruction being decoded is a beqjalr

Given the single cycle datapath below, select the correct modifications in parts such that the datapath executes correctly for this new instruction (and all other instructions!). You can make the following assumptions:

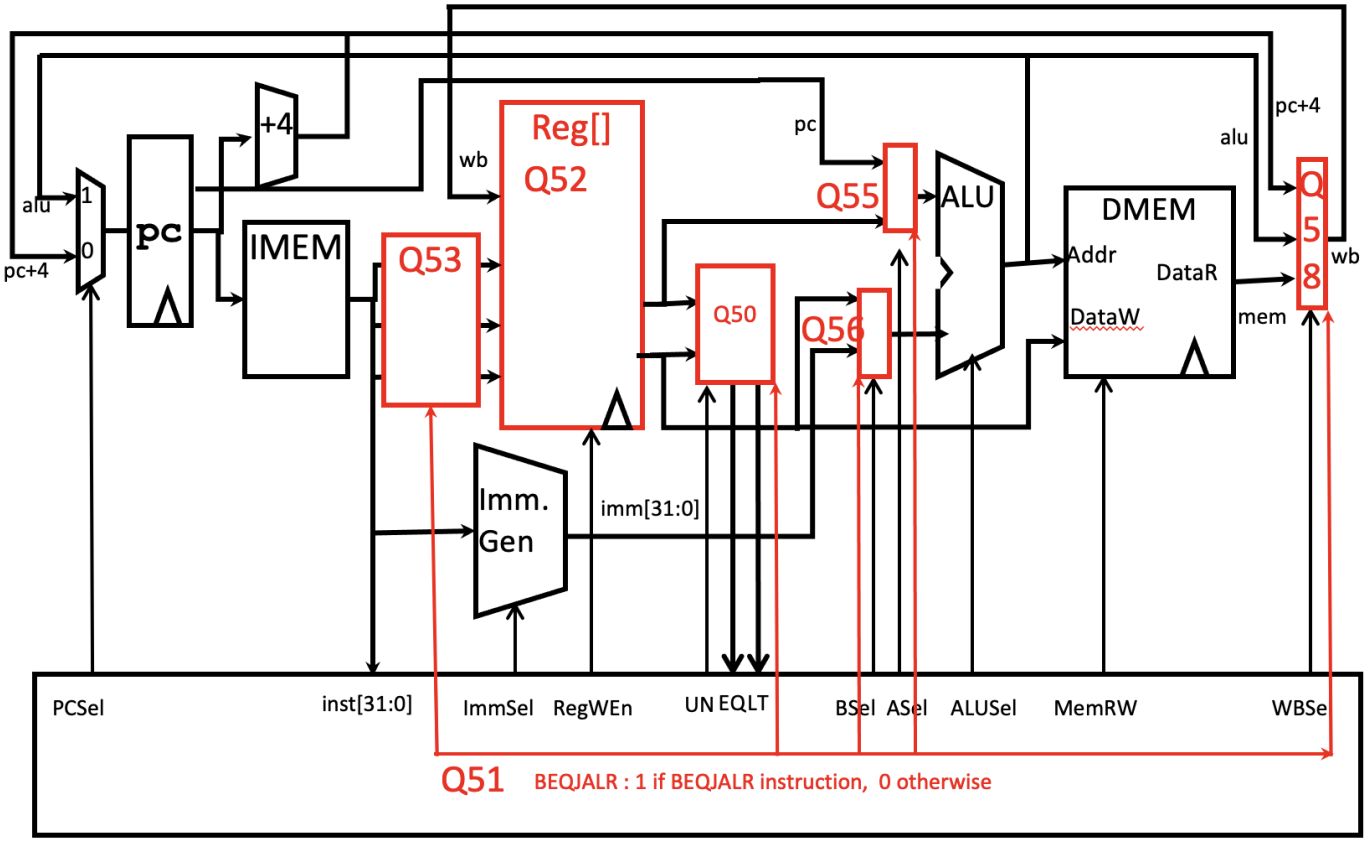
`Caution 2: Pay careful attention to which input line is 1 and which line is 0 in the muxes. Some muxes choose top-most input as 0, some choose bottom-most input as 0`

`Hint: YOU DO NOT REQUIRE TRUTH TABLES`
`Try writing down in plain english or reading out the logic`
`to yourself e.g, !(A<=B) is A is not equal to B and A is not LT (less than) B`

Baseline Pipeline



Pipeline with beqjalr (Red boxes indicate questions)



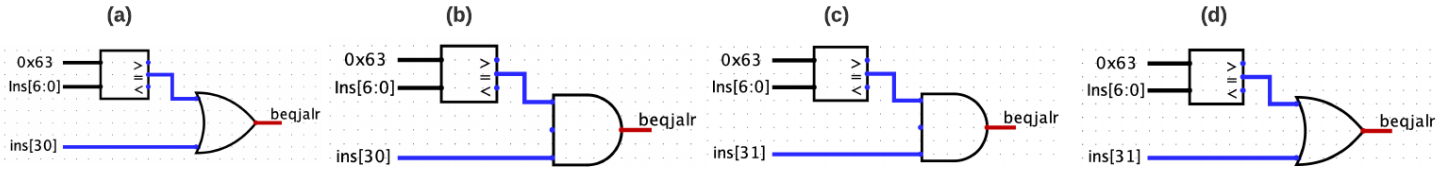
47. What is the number of register that beqjalr needs to read and write in a single cycle ? (1)

48. What is the RegWEn signal ? (1)

49. What is the branch comparison signal we are interested in? (1)

50. Which fields are passed to the branch comparison ? (1)

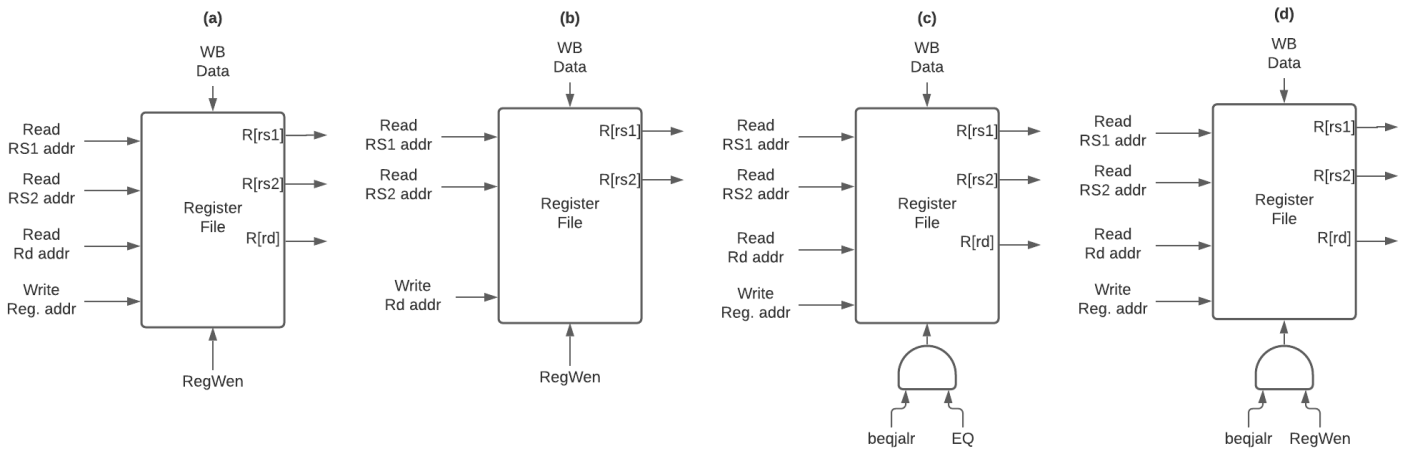
51. What is the logic for beqjalr signal ? (1)



52. Consider the following modifications to the Reg[] register file. (2)

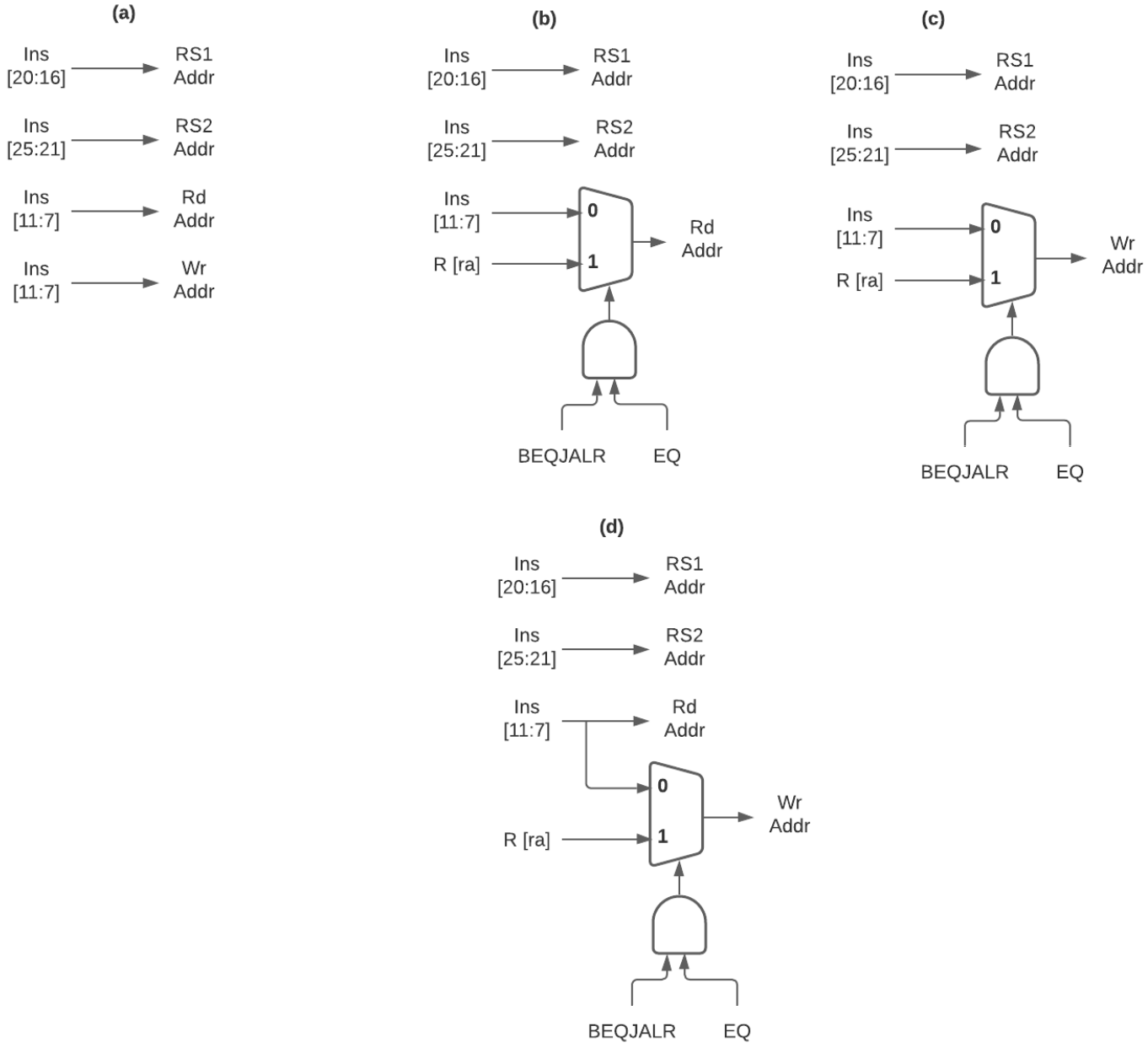
Which configuration will allow this instruction to execute correctly without breaking the execution of other instructions in our instruction set?

EQ is 1 if R[rs1]==R[rs2]. 0 otherwise



53. What are the inputs to the register file ? (2)

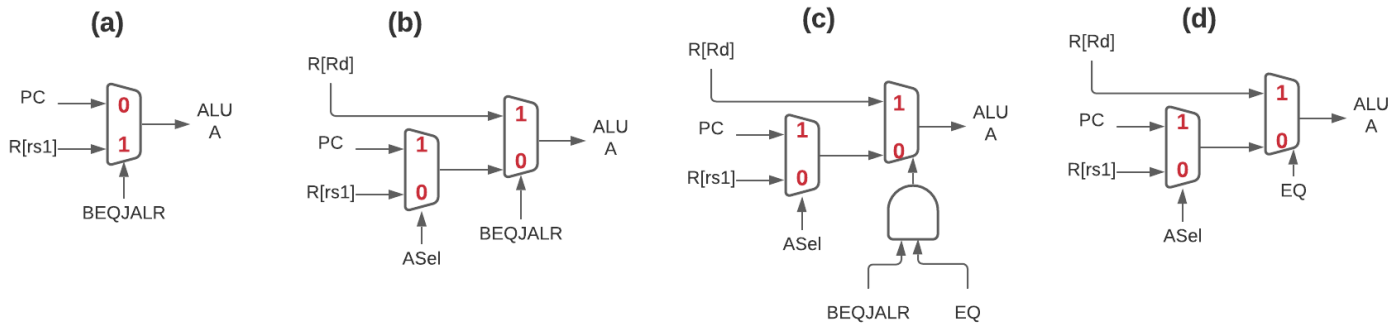
Which configuration will allow this instruction to execute correctly without breaking the execution of other instructions in our instruction set?



54. What are the inputs to the ALU ? (1)

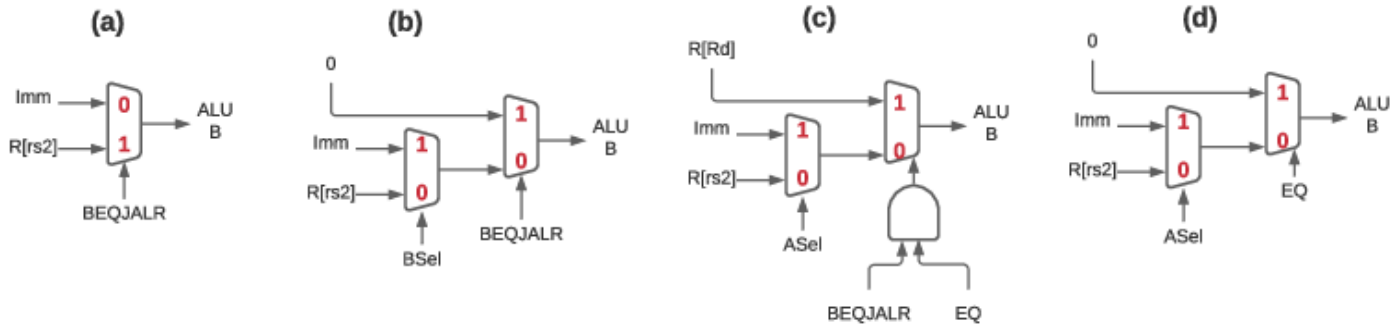
55. What are the changes to mux-A ? (2)

Which configuration will allow this instruction to execute correctly without breaking the execution of other instructions in our instruction set?



56. What are the changes to mux-B ? (2)

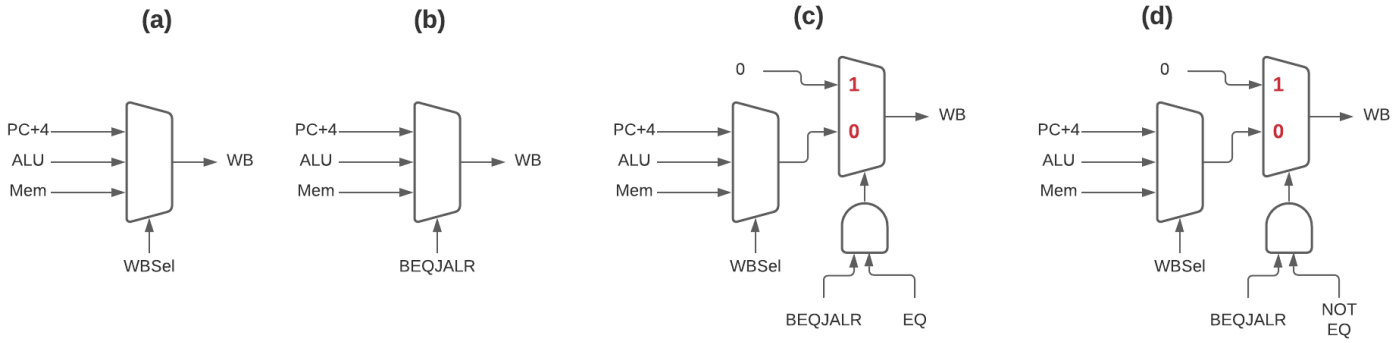
Which configuration will allow this instruction to execute correctly without breaking the execution of other instructions in our instruction set?



57. For beqjalr instruction which signal does WBsel choose ? (2)

Which configuration will allow this instruction to execute correctly without breaking the execution of other instructions in our instruction set?

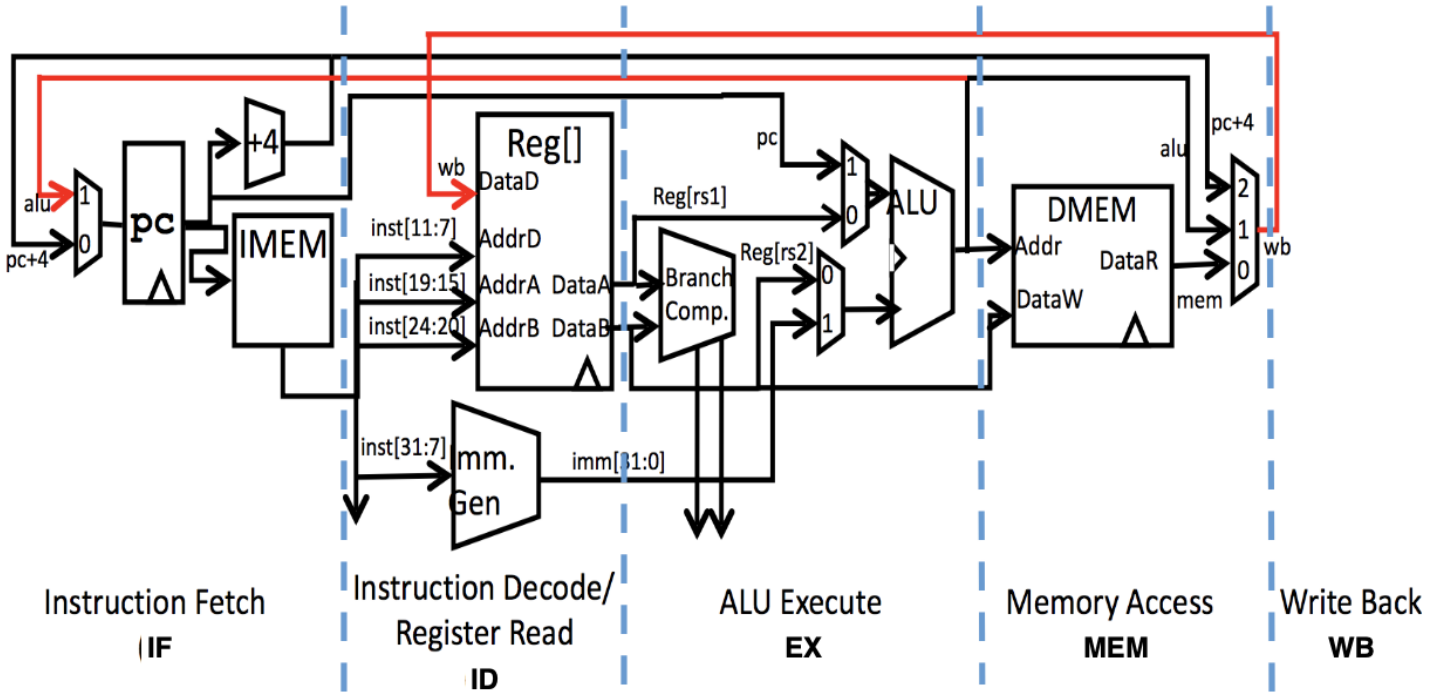
58. What are the changes to the writeback stage ? (2)



F. RISC-V Pipeline 12 points.

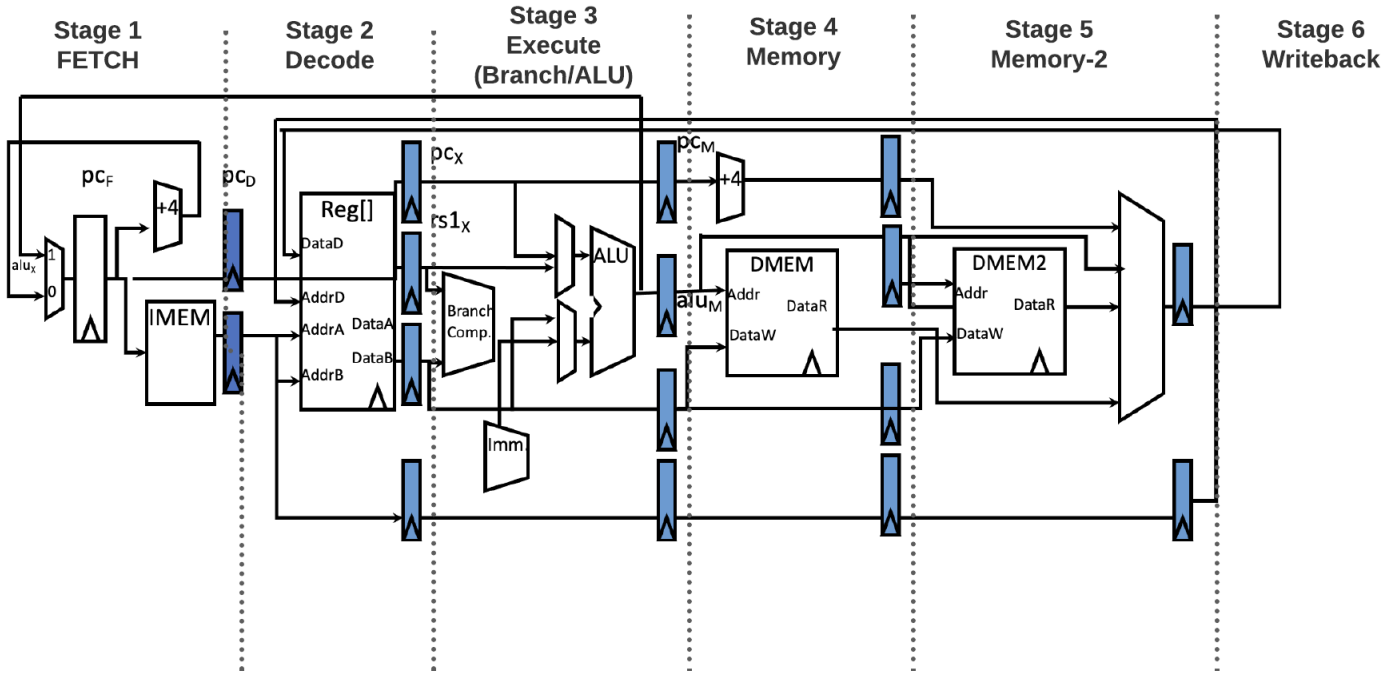
`Refer slide deck L29-Hazard Week 11 if you need to.`

Consider a typical 5-stage (Fetch,Decode,EXecute,Memory,WriteBack) pipeline.Assume pipeline registers exist where the dotted lines are



This pipeline is more simple than the one you dealt with in the assignment. `READ RULES BELOW`

- Forwarding/Bypassing is not implemented; dependent instructions will have to wait for WB to complete.
- Following a branch, the next instructions stalls until branch is resolved..
- A stall is the number of cycles after the previous instruction that the current instruction can start. We
- modify this pipeline to add another memory stage and create a six-stage pipeline.



Answer questions based on the following program

For the given code, what hazards might exist and due to which lines? Assume all registers have been initialised and that all labels are defined and that all branches are taken

```
1  bneq a0,zero,end
2  addi t0,t0,1
3  lw   s0,0x10(t0)
4  mul  s1,s0,a0
5  add  s1,s0,a0
```

59. What hazards existing between instruction 1 and 2 ? (1)

60. What hazards existing between instruction 2 and 3 ? (1)

61. What hazards existing between instruction 3 and 4 ? (1)

62. What hazards existing between instruction 4 and 5 ? (1)

63. How many cycles does instruction 2 stall for ? (2)

64. How many cycles does instruction 3 stall for ? (2)

65. How many cycles does instruction 4 stall for ? (2)

66. How many cycles does instruction 5 stall for ? (2)

G. Lets RISC-V II 10 points

67. We are designing a new RISC-V instruction with 16 registers. Assuming that you use the extra bits to extend the immediate field, what is the range of `half-word` instructions that can be reached using a branch instruction in this new format? (2)

Refer code below for remaining questions

```
1  add s0, x0, x0
2  addi s1, x0, 4
3  loop:
4    beq s0, s1, end
5    add a0, a0, s0
6    jal ra, square
7    jal ra, printf
8  n:
9    addi s0, s0, 1
10   j loop
11 end:
12   ecall
13 square:
14   mul a0, a0, a0
15   ret
```

68. What is the PC address of `instruction 4:beq` (hex) ?

69. What is the PC address of `instruction 9:addi` (hex) ?

70. What is the PC address of `instruction 12:ecall` (hex) ?

71. What is the PC address of `instruction 14:mul` (hex) ?

72. What is the machine code for instruction at address 0x1C (hex) ? (2)

73. After the first pass of the assembler instruction at 0d20 does not have the label resolved. (1)

74. After the first pass of the assembler instruction at 0d28 does not have the label resolved. (1)

dec	oct	hex	ch	dec	oct	hex	ch	dec	oct	hex	ch
32	40	20	(space)	64	100	40	@	96	140	60	`
33	41	21	!	65	101	41	A	97	141	61	a
34	42	22	"	66	102	42	B	98	142	62	b
35	43	23	#	67	103	43	C	99	143	63	c
36	44	24	$	68	104	44	D	100	144	64	d
37	45	25	%	69	105	45	E	101	145	65	e
38	46	26	&	70	106	46	F	102	146	66	f
39	47	27	'	71	107	47	G	103	147	67	g
40	50	28	(	72	110	48	H	104	150	68	h
41	51	29	)	73	111	49	I	105	151	69	i
42	52	2a	*	74	112	4a	J	106	152	6a	j
43	53	2b	+	75	113	4b	K	107	153	6b	k
44	54	2c	,	76	114	4c	L	108	154	6c	l
45	55	2d	-	77	115	4d	M	109	155	6d	m
46	56	2e	.	78	116	4e	N	110	156	6e	n
47	57	2f	/	79	117	4f	O	111	157	6f	o
48	60	30	0	80	120	50	P	112	160	70	p
49	61	31	1	81	121	51	Q	113	161	71	q
50	62	32	2	82	122	52	R	114	162	72	r
51	63	33	3	83	123	53	S	115	163	73	s
52	64	34	4	84	124	54	T	116	164	74	t
53	65	35	5	85	125	55	U	117	165	75	u
54	66	36	6	86	126	56	V	118	166	76	v
55	67	37	7	87	127	57	W	119	167	77	w
56	70	38	8	88	130	58	X	120	170	78	x
57	71	39	9	89	131	59	Y	121	171	79	y
58	72	3a	:	90	132	5a	Z	122	172	7a	z

58	72	3a	:	90	132	5a	Z	122	172	7a	z
59	73	3b	;	91	133	5b	[	123	173	7b	{
60	74	3c	<	92	134	5c	\	124	174	7c	|
61	75	3d	=	93	135	5d	]	125	175	7d	}
62	76	3e	>	94	136	5e	^	126	176	7e	~
63	77	3f	?	95	137	5f	_	127	177	7f	**DEL** (delete)