HONOR CODE

- I have not used any online resources during the exam.
- I have not obtained any help either from anyone in the class or outside when completing this exam.
- No sharing of notes/slides/textbook between students.
- **Canvas answers may be locked after 1st try in case of snafus; so fill out after you work out on paper**

Questions Sheet.

Read all of the following information before starting the exam:

- For each question fill out the appropriate choice or write text on page. Also type clearly on in the exam on the appropriate text.
- IF THE MULTIPLE CHOICE ANSWER IS WRONG WE WILL MARK THE ANSWER WRONG. IF THE MULTIPLE-CHOICE ANSWER IS CORRECT, WE WILL READ THE WRITTEN PORTION.
- 1 pt Qs (0 or 1). 2 or 3pt Qs (if no explaination only 1 pt.)
- Show all work, clearly and in order, if you want to get full credit.
- We reserve the right to take off points if we cannot see how you logically got to the answer (even if your final answer is correct). 1 or 2 sentences atmost.
- I will take points off for rambling and for incorrect or irrelevant statements.

Canvas Rules

- On canvas only write the answer. We autograde so extra text will throw off the autograder.
- Always use lower case and prefix 0x for hex.

  `Correct: 0xabcdef Incorrect: 0xABCDEF`
- No leading zeros e.g., `Correct: 0xa Incorrect: 0x0a`
- Paper/PDF includes details and hints that will help with answering. Canvas only lists question.

- HONOR CODE
- Questions Sheet.
- Canvas Rules
- A Virtual Memory [15]. Canvas Q1-Q28
  - Common questions. Canvas Q1-Q2
  - For the virtual address 0x15957 answer the following Canvas Q3-Q12. All in hex. (0.5 pt each)
  - For the virtual address 0x2ee19 answer the following. Canvas Q13-Q22. All in hex (0.5 pt each)
  - For the virtual address 0x1a344 answer the following. All in hex (Canvas: 23-28) (0.5 pt each)
- B. Easy. RISCV Blackbox. [10]
  - Answer questions below for the code shown.
  - 29. _____ bytes are stored to memory? [1]
  - 30. The string result is "___" ? [1]
  - Answer questions below for the code shown.
  - 31. _____ bytes are stored to memory? [1]
  - 32. The string result is _____ ? [2]
  - Answer questions below for the code shown.
  - 33. _____ bytes are stored to memory? [2]
  - 34. The string result is _____ ? [3]
- C. Lets Cache I [14]
  - 35. The hit ratio of loop 1 for Cache A is _____ ? (1)
  - 36. The hit ratio of loop 1 for Cache B is _____ ? (1)
  - 37. The hit ratio of loop 2 for Cache A is _____ (loop 1 has run) ? (1)
  - 38. The hit ratio of loop 2 for Cache B is _____ (loop 1 has run) ? (1)
  - 39. The hit ratio of loop 3 for Cache A is _____ (loop 1 and 2 have run) ? (2)
  - 40. The hit ratio of loop 3 for Cache B is _____ (loop 1 and 2 have run) ? (2)
  - 41. The hit ratio if loop 3 changes to below (on Cache A) ? (2)
  - 42. What is the hit ratio if loop 3 is same as Q41. (on Cache B) ? (2)
  - 43. What is hit ratio for the code below. Assume Cache B ? (2)
- D. RISC-V Single Cycle Datapath [15]
  - 44. What is the logic for badd signal ? (1)
  - 45. _ is the number of registers badd needs to access in a single cycle ? (1)
  - 46. What is the RegWen signal for `badd` ? (1)
  - 47. What is the comparison logic we are interested in ? (2)
  - 48. Consider the following modifications to the Reg[] register file. (2)
  - 49. What is ASel and BSel (2)
  - 50. What are the changes to mux-A ? (2)
  - 51. What are the changes to mux-B ? (2)
  - 52. The WBsel select is _ ? (2)
- E. RISC-V Pipeline [17].

- Part 1
  - 53. What hazards existing between line 3 and 4 ? (1)
  - 54. What hazards existing between line 4 and 5 ? (1)
  - 55. What is the instruction in IF stage t = 6 ?
  - 56. What is the instruction in IF stage of t = 7 ?
  - 57. How many cycles does this program take to complete (Part 1)?
- Part 2.
  - 58. What is the instruction in IF stage t = 6 ?
  - 59. What is the instruction in IF stage of t = 7 (Part 2) ?
  - 60. How many cycles does this program take to complete (Part 2) ?
- Part 3.
  - 61. What is the instruction in IF stage t = 6 (Part 3)?
  - 62. What is the instruction in IF stage of t = 7 (Part 3)?
  - 63. How many cycles does this program take to complete (Part 3)?
- Part 4.
  - 64. What is the instruction in IF stage t = 6 ?
  - 65. How many cycles does this program take to complete (Part 4) ?

- F. Pipeline CPU. [4]
  - 66. Assuming that this CPU is NOT Pipelined (i.e. it is a single cycle CPU), what is the shortest clock period possible to execute the instruction? _____
  - 67. Assuming that this CPU is pipelined, what is the shortest clock period possible to execute the instruction? _____

-

A Virtual Memory [15]. Canvas Q1-Q28

```
Refer slide deck L21-VM-III Week 8 if you need to.
```

The chart below shows how memory accesses are treated in a system. The table below describes the parameters int he memory system.
Please use the data below to answer question groups Q1,Q2,Q3,Q4 on canvas.

```
CAUTION 1: When converting from binary to hex you can always pad the MSB
e.g., 10 1010 (6 bit field) in hex is 0010 1010 (2 0s padded in MSB)
is 0x2a .

always use lower case and prefix 0x for hex .
Correct: 0xabcdef Incorrect: 0xABCDEF
```

Parameter	Value
Physical address bits	18
Size of page	64 bytes
Virtual address bits	18
----------	----------
TLB Sets	8
TLB Ways	2
----------	----------
Cache size	256 bytes
Cache Sets	16
Cache Ways	2

- VPN - Virtual page number
- Index (Set index of cache or TLB)
- PPN - Physical page number
- INVALID. TLB entry is invalid

- TLB-T (TLB Tag)

TLB

Way 0	TLB-T	PPN
Set 0	[0x1cb]	0x958
Set 1	[0x1be]	---
Set 2	[0xa4]	0xe76
Set 3	[0x74]	----
Set 4	[0x11d]	0x2b5
Set 5	[0xbc]	0xa36
Set 6	[0x1fb]	---
Set 7	[0xf1]	0xfea

Way 0	TLB-T	PPN
Set 0	[0x177]	0x47b
Set 1	[0x24]	---
Set 2	[0x12]	0x84a
Set 3	[0x16c]	---
Set 4	[0x192]	0xe76
Set 5	[0xd1]	---
Set 6	[0xab]	0xec3
Set 7	[0xc6]	---

Page Table (Partial)

```
CAUTION: Only partial table relevant to the questions are shown.
```

VPN	PPN	Valid
0xbb8	0x47b	1
0xe58	0x958	1
0x522	e76	1
0xdf1	---	0
0xfde	---	0
0x78f	fea	1
0x383	0xa3	1
0x68d	---	0
0x565	0x636	1

Cache

Way 0	Tag	0	1	2	3	4	5	6	7
Set 0	[0x322]	0x13	0xc8	0xce	0xc6	0x76	0x7c	0xde	0xf3
Set 1	[0x45a]	0xbc	0x0f	0xd8	0x93	0xe7	0x69	0xea	0xb1
Set 2	[0x6f6]	0x56	0xf3	0x3d	0xd6	0x7b	0x2c	0x98	0x34
Set 3	[0x276]	0xf3	0x8c	0x94	0x8d	0xaf	0x5c	0x02	0x3b
Set 4	[0x23c]	0x3a	0x09	0x3c	0x3b	0x35	0x3f	0x85	0x1e
Set 5	[0x425]	0x19	0x65	0xaf	0x3e	0xb4	0x8a	0x8a	0xcf
Set 6	[0x62e]	0x88	0x87	0xad	0x73	0xac	0x70	0xeb	0x77
Set 7	[0x4ac]	0x0c	0x02	0x16	0xfe	0x7b	0x34	0xd6	0x91
Set 8	[0x761]	0xc9	0x97	0x01	0x6d	0xea	0x55	0x59	0x73
Set 9	[0x242]	0xe2	0x55	0x38	0xd0	0x84	0x6c	0x16	0x5b
Set 10	[0x494]	0x76	0x78	0x19	0x6b	0xb6	0xf3	0xa4	0xfb
Set 11	[0x23d]	0xf5	0xac	0x7f	0xf5	0x1f	0xb8	0x03	0x20
Set 12	[0x7b9]	0x11	0x9a	0xd4	0x8d	0x85	0xe8	0xb3	0xb1
Set 13	[0x15a]	0x4e	0xaa	0x51	0x0f	0x61	0xc3	0x8f	0x0e
Set 14	[0x739]	0x77	0x71	0x3b	0xb8	0xa7	0x70	0x18	0x15
Set 15	[0x627]	0x7f	0x65	0xe0	0x34	0x1a	0x90	0xb5	0x19

Way 1	Tag	0	1	2	3	4	5	6	7
Set 0	[0x7f5]	0x11	0xbf	0xe8	0x3e	0xad	0x26	0x2e	0xaa
Set 1	[0x73b]	0xe3	0x08	0x0b	0x3a	0xc6	0x98	0x67	0x17
Set 2	[0x31b]	0x39	0x16	0x2e	0xbc	0xde	0x90	0xb5	0x61
Set 3	[0x755]	0x2b	0x39	0x46	0xf5	0x95	0xb7	0x43	0x6d
Set 4	[0x627]	0x51	0x8f	0x28	0xb4	0x1d	0xac	0x8c	0x3d
Set 5	[0x2af]	0xf5	0x49	0x67	0x1d	0xcb	0x75	0x8e	0x05
Set 6	[0xf2]	0xc1	0xcd	0x99	0xce	0x27	0xb1	0x9b	0xaf
Set 7	[0x236]	0xbb	0xe4	0xda	0xcd	0x43	0xa6	0xa0	0x11
Set 8	[0x1c1]	0x02	0x29	0xe3	0x33	0xa9	0x24	0x89	0x1e
Set 9	[0x335]	0x32	0x44	0x68	0x76	0x7b	0xfb	0x7d	0xc9
Set 10	[0x64]	0x3c	0x84	0x70	0x27	0x98	0x88	0x96	0x73
Set 11	[0x51]	0x50	0x82	0x6c	0xda	0x93	0x3a	0x77	0x8b
Set 12	[0x56f]	0x9c	0xd1	0xc7	0xba	0x62	0xde	0x1e	0x37
Set 13	[0x654]	0xd5	0x9c	0x66	0x8f	0x95	0xa6	0x3f	0x4c
Set 14	[0x1e4]	0xc9	0x96	0xb0	0x3b	0xfb	0x76	0xa3	0x77
Set 15	[0x5d8]	0xb3	0x4f	0x91	0xe9	0x6e	0xa5	0x91	0x8a

Common questions. Canvas Q1-Q2

1. How many bits is the VPN. decimal (1pt) ?

2. How many bits is the PPN. decimal (1pt) ?

For the virtual address 0x15957 answer the following Canvas Q3-Q12. All in hex. (0.5 pt each)

- What is the VPN

- What is the TLB tag.

- Is it a TLB hit or miss
  - Hit
  - Miss
  - N/A

- Is it a page fault
  - Yes
  - No
  - N/A
- What is the PPN ?

- what is the cache tag ?

- what is the cache index

- What is the byte offset

- Is it a cache hit or miss
  - Hit
  - Miss
  - N/A
- What is the data byte

For the virtual address 0x2ee19 answer the following. Canvas Q13-Q22. All in hex (0.5 pt each)

- What is the VPN

- What is the TLB tag.

- Is it a TLB hit or miss
  - Hit
  - Miss
  - N/A
- Is it a page fault
  - Yes
  - No
  - N/A
- What is the PPN ?

- what is the cache tag ?

- what is the cache index

- What is the byte offset

- Is it a cache hit or miss
  - Hit
  - Miss
  - N/A
- What is the data byte

For the virtual address 0x1a344 answer the following. All in hex (Canvas: 23-28) (0.5 pt each)

- What is the VPN

- What is the TLB tag.

- Is it a TLB hit or miss
  - Hit
  - Miss
  - N/A
- Is it a page fault
  - Yes
  - No
  - N/A
- What is the PPN ?

- Is it a cache hit ?
  - Hit
  - Miss
  - N/A

B. Easy. RISCV Blackbox. [10]

`WARNING: FOR THIS QUESTION MAKE SURE YOU WRITE YOUR CORRECT ANSWER AT THE BEGINNING.`

Assume we have two arrays input and result.
`a0=message, a1=result` . Answer questions below.

```
1 char *message = "ABCDE"
2 char result[20];
```

Answer questions below for the code shown.

```
1   lbu  s0 0(a0)
2   slli s1 s0 8
3   add  s1 s1 s0
4   sh   s1 0(a1)
```

29. _____ bytes are stored to memory? [1]

30. The string result is "___" ? [1]

Answer questions below for the code shown.

```
1 BLACKBOX:
2   lbu  s0 0(a0)
3   slli s1 s0 8
4   addi s0 s0 1
5   add  s1 s1 s0
6   slli s2 s1 16
7   add s2 s2 s0
8   sw   s2 0(a1)
```

31. _____ bytes are stored to memory? [1]

32. The string result is _____ ? [2]

Answer questions below for the code shown.

```
1  .text
2  BLACKBOX:
3    lbu  s0 0(a0)
4    beq  s0 x0 End
5    slli s1 s0 8
6    add  s1 s1 s0
7    sh   s1 0(a1)
8    sb   s0 2(a1)
9    addi a0 a0 1
10   addi a1 a1 3
11 j BLACKBOX
12 end:
13   sb x0 0(a1)
```

33. _____ bytes are stored to memory? [2]

34. The string result is _____ ? [3]

C. Lets Cache I [14]

We will be studying the behavior of different loops on two different caches.

Cache-A	Direct-mapped, 4KB, 64 sets
Cache-B	Set-associate, 4KB, 2 ways, 32 sets

Both caches use write-back and write-allocate policies.
Hit ratio is written as #Hits:#Accesses
Hit-Miss ratio is: #Hits:#Misses
Hit % : #Hits:#Accesses * 100.

Answer questions below

```
int size = 4096;
// int is 4 bytes
int a[size];
// long long int is 8 bytes
long long int a_long[size];

/* loop 1 */
for (int i = 0; i < size; i++) {
  a[i] = i;
}
/* loop 2 */
for (int i = 0; i < size; i++) {
  a_long[i] = i;
}

/* loop 3 */
for (int i = 0; i < size/2; i += 1) {
  a[(size/2)+i] = a[i];
}
```

35. The hit ratio of loop 1 for Cache A is _____ ? (1)

Write it as Hits:Accesses

36. The hit ratio of loop 1 for Cache B is _____ ? (1)

37. The hit ratio of loop 2 for Cache A is _____ (loop 1 has run) ? (1)

38. The hit ratio of loop 2 for Cache B is _____ (loop 1 has run) ? (1)

39. The hit ratio of loop 3 for Cache A is _____ (loop 1 and 2 have run) ? (2)

Hint: write down which array elements loop 3 touches and think which sets they map to.

40. The hit ratio of loop 3 for Cache B is _____ (loop 1 and 2 have run) ? (2)

41. The hit ratio if loop 3 changes to below (on Cache A) ? (2)

```
/* loop 3 */
for (int i = 0; i < size/2; i += 4) {
int tmp0 = a_int[i+0]
int tmp1 = a_int[i+1]
int tmp2 = a_int[i+2]
int tmp3 = a_int[i+3]
a_int[size/2+(i+0)] = tmp0
a_int[size/2+(i+1)] = tmp1
a_int[size/2+(i+2)] = tmp2
a_int[size/2+(i+3)] = tmp3
}
```

42. What is the hit ratio if loop 3 is same as Q41. (on Cache B) ? (2)

43. What is hit ratio for the code below. Assume Cache B ? (2)

```
struct int_and_long {
  int a_int;
  long long int a_long;
};
int size = 4096;
// int is 4 byte aligned
// long long int is 8 byte aligned
struct int_and_long s[4096];

/* loop 1 */
for (int i = 0; i < size/2; i += 1) {
  s[size-1-i].a_int = s[i].a_int
}
```

D. RISC-V Single Cycle Datapath [15]

We wish to introduce a new instruction into our RISC-V datapath.
`badd` (branch and add). This instruction is a conditional add instruction. The instruction works as follows. The instruction is encoded as follows.

`Add instruction`

						Opcode
f7	rs2	rs1	0x0	f3	rd	0110011

`new badd instruction`

0x10	rs2	rs1	0x0	f3	rd	0001011

```
if (R[rs1] > R[rs2]) {
  R[rd]++
} else  {
 R[rd] = R[rd]
}
```

It combines the semantics of branch and R-type instruction.

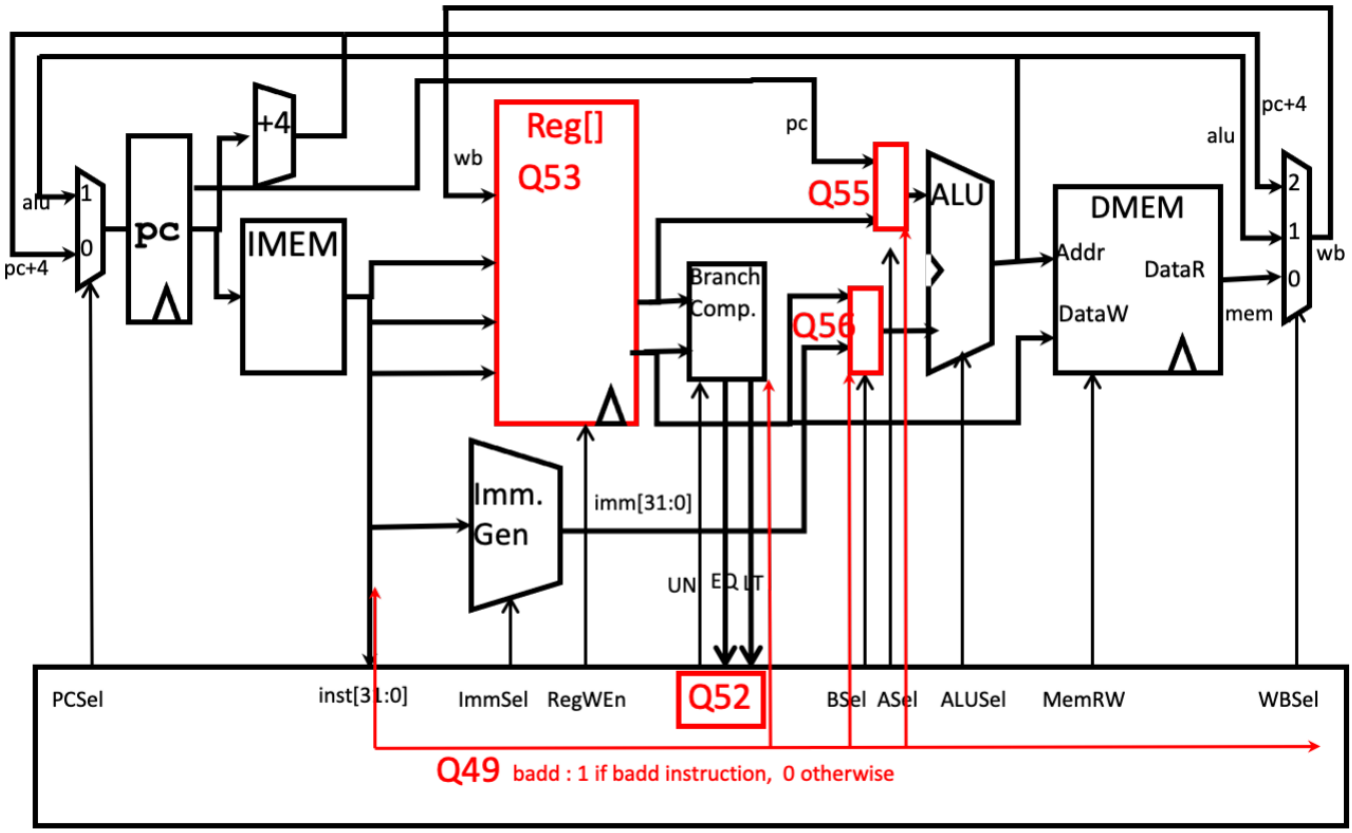
- Like a branch it performs a comparison.
- If comparison succeeds it increments rd. rd is destination and source.
- If comparison fails, it simply retains the value in R[rd].
- We have a new control signal `badd` which is 1 if the instruction being decoded is a badd.

Given the single cycle datapath below, select the correct modifications in parts such that the datapath executes correctly for this new instruction (and all other instructions!). You can make the following assumptions:

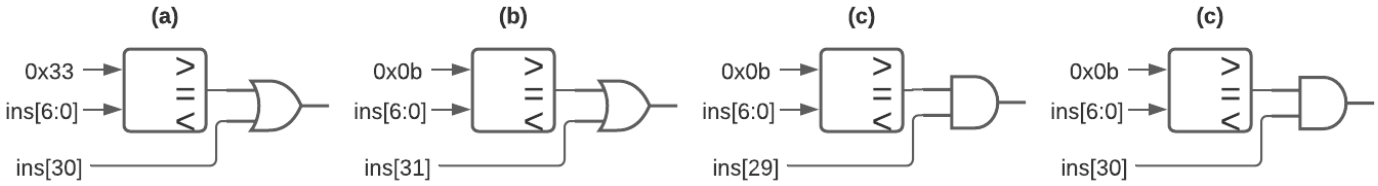
`Caution 2: Pay careful attention to which input line is 1 and which line is 0 in the muxes. Some muxes choose top-most input as 0, some choose bottom-most input as 0`

`Hint: YOU DO NOT REQUIRE TRUTH TABLES`
`Try writing down in plain english or reading out the logic`
`to yourself e.g, !(A<=B) is A is not equal to B and A is not LT (less than) B`

Pipeline with badd (Red boxes indicate questions)



44. What is the logic for badd signal ? (1)



45. _ is the number of registers badd needs to access in a single cycle ? (1)

46. What is the RegWen signal for `badd` ? (1)

[ ] 0

[ ] 1

[ ] Don't Care

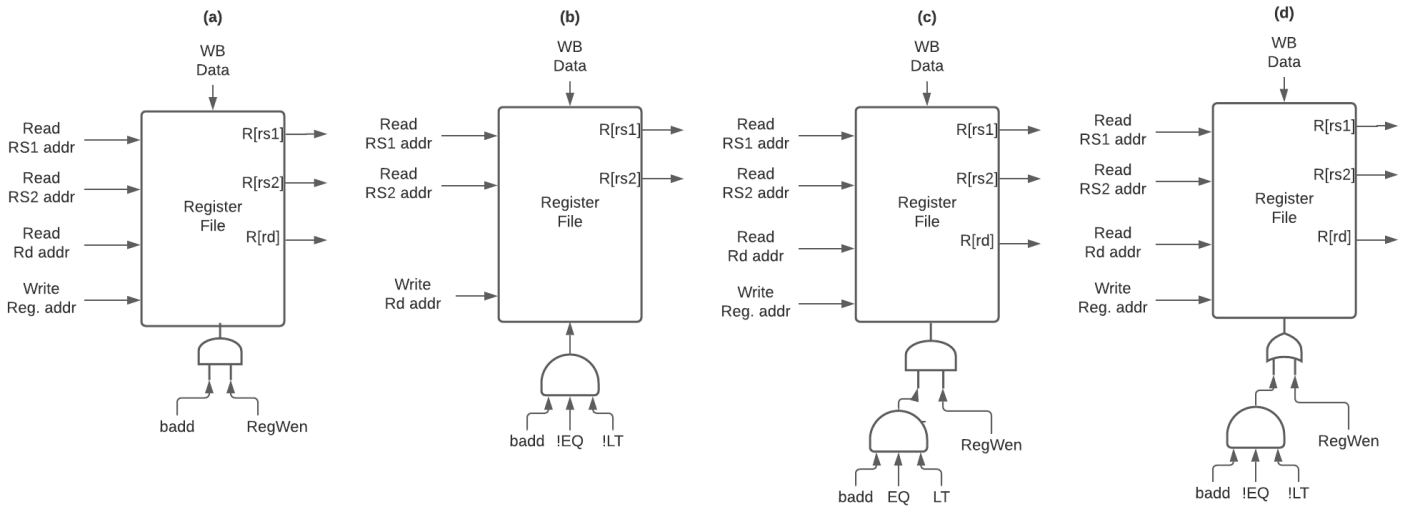
47. What is the comparison logic we are interested in ? (2)

! = Not operator.

[ ] EQ OR NT
[ ] EQ AND NT
[ ] !EQ AND !NT
[ ] !(EQ AND NT)

48. Consider the following modifications to the Reg[] register file. (2)

all instructions have to run correctly.

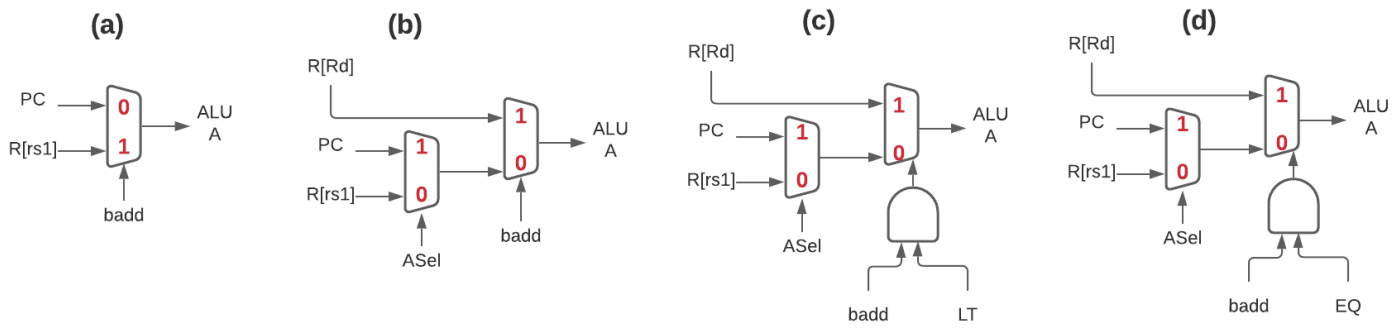


49. What is ASel and BSel (2)

[ ] 0
[ ] 1
[ ] Don't Care

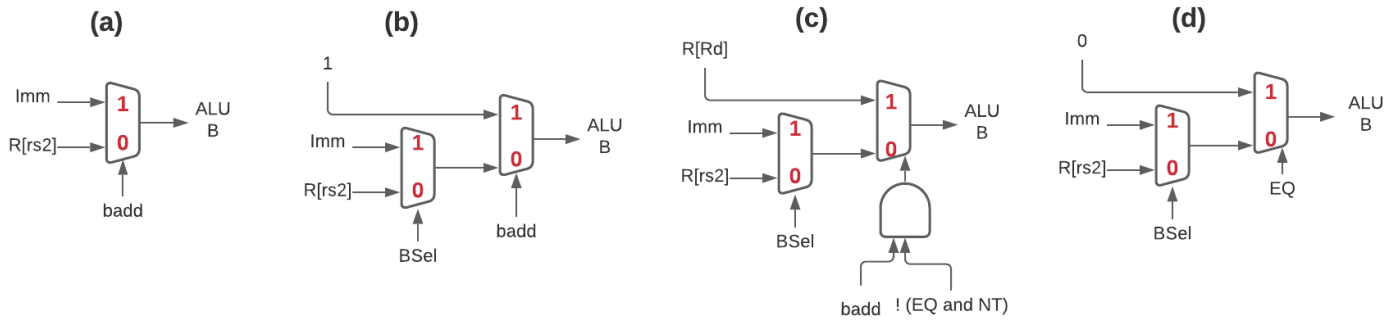
50. What are the changes to mux-A ? (2)

all instructions have to run correctly.



51. What are the changes to mux-B ? (2)

all instructions have to run correctly.



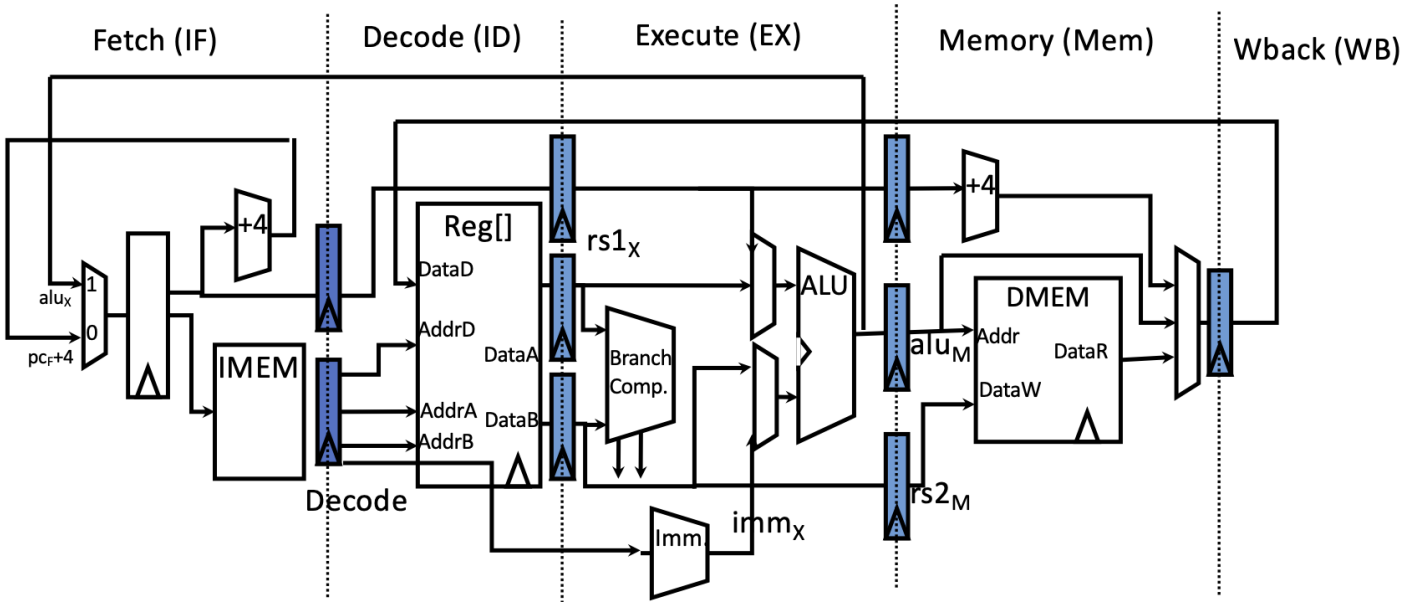
52. The WBsel select is _ ? (2)

[ ] ALU
[ ] PC+4
[ ] Mem

E. RISC-V Pipeline [17].

`Refer slide deck L29-Hazard Week 11 if you need to.`

Consider a typical 5-stage (Fetch,Decode,EXecute,Memory,WriteBack) pipeline.Assume pipeline registers exist where the dotted lines are



Typo: 55 and 56 above refer to 51 and 50

READ RULES BELOW

- Pipeline similar to the one you played with in Assignment 6
- Forwarding/Bypassing is implemented.
- Branches targets are calculated in the EX stage.
- Branch comparison in the EX stage.
- We can read and write the register in a cycle.
- A stall is the number of extra cycles an instruction wastes cause of a hazard.
- Assume at t=0 instruction 1 is in the pipeline. is in IF stage when calculating cycles below.

Part 1

```
if (a0 == 1) {
   // Choice 1
} else if (a0 == 2) {
   // Choice 2
} else if (a0 == 3) {
  // Choice 3
}
```

The assembly code below implements the following

```
1  main:
2    addi a0,zero,1
3    addi t1,t1,1
4    beq  a0,t1,choice1
5    addi t1,t1,1
6    beq  a0,t1,choice2
7    addi t1,t1,1
8    beq  a0,t1,choice3
9
10 choice1: # Jumped into choice 1
11         j end
12 choice2:  # Jumped into choice 2.
13   j end
14 choice3:
15   j end
16 end:
17   addi a0, zero, 10
18   ecall # terminate ecall
```

53. What hazards existing between line 3 and 4 ? (1)

[ ] Data

[ ] Control

[ ] Structural

[ ] Memory

54. What hazards existing between line 4 and 5 ? (1)

[ ] Data
[ ] Control
[ ] Structural
[ ] Memory

55. What is the instruction in IF stage t = 6 ?

[ ] 3: addi t1,t1,1
[ ] 4: beq a0,t1,choice1
[ ] 5: addi t1,t1,1
[ ] 6: beq a0,t1,choice2
[ ] 7: addi t1,t1,1
[ ] 8: beq a0,t1,choice3
[ ] 11: j end
[ ] 13: j end
[ ] 15: j end
[ ] 17: addi a0, zero, 10
[ ] 18: ecall

56. What is the instruction in IF stage of t = 7 ?

[ ] 3: addi t1,t1,1
[ ] 4: beq a0,t1,choice1
[ ] 5: addi t1,t1,1
[ ] 6: beq a0,t1,choice2
[ ] 7: addi t1,t1,1
[ ] 8: beq a0,t1,choice3
[ ] 11: j end
[ ] 13: j end
[ ] 15: j end
[ ] 17: addi a0, zero, 10
[ ] 18: ecall

57. How many cycles does this program take to complete (Part 1)?

Part 2.

For questions below assume we have changed line 2 to **addi a0,zero,2** i.e., we are going into choice 2.

58. What is the instruction in IF stage t = 6 ?

[ ] 3: addi t1,t1,1
[ ] 4: beq a0,t1,choice1
[ ] 5: addi t1,t1,1
[ ] 6: beq a0,t1,choice2
[ ] 7: addi t1,t1,1
[ ] 8: beq a0,t1,choice3
[ ] 11: j end
[ ] 13: j end
[ ] 15: j end
[ ] 17: addi a0, zero, 10
[ ] 18: ecall

59. What is the instruction in IF stage of t = 7 (Part 2) ?

[ ] 3: addi t1,t1,1
[ ] 4: beq a0,t1,choice1
[ ] 5: addi t1,t1,1
[ ] 6: beq a0,t1,choice2
[ ] 7: addi t1,t1,1
[ ] 8: beq a0,t1,choice3
[ ] 11: j end
[ ] 13: j end
[ ] 15: j end
[ ] 17: addi a0, zero, 10
[ ] 18: ecall

60. How many cycles does this program take to complete (Part 2) ?

Part 3.

For questions below assume we have changed line 2 to **addi a0,zero,3** i.e., we are going into choice 3

61. What is the instruction in IF stage t = 6 (Part 3)?

[ ] 3: addi t1,t1,1
[ ] 4: beq a0,t1,choice1
[ ] 5: addi t1,t1,1
[ ] 6: beq a0,t1,choice2
[ ] 7: addi t1,t1,1
[ ] 8: beq a0,t1,choice3
[ ] 11: j end
[ ] 13: j end
[ ] 15: j end
[ ] 17: addi a0, zero, 10
[ ] 18: ecall

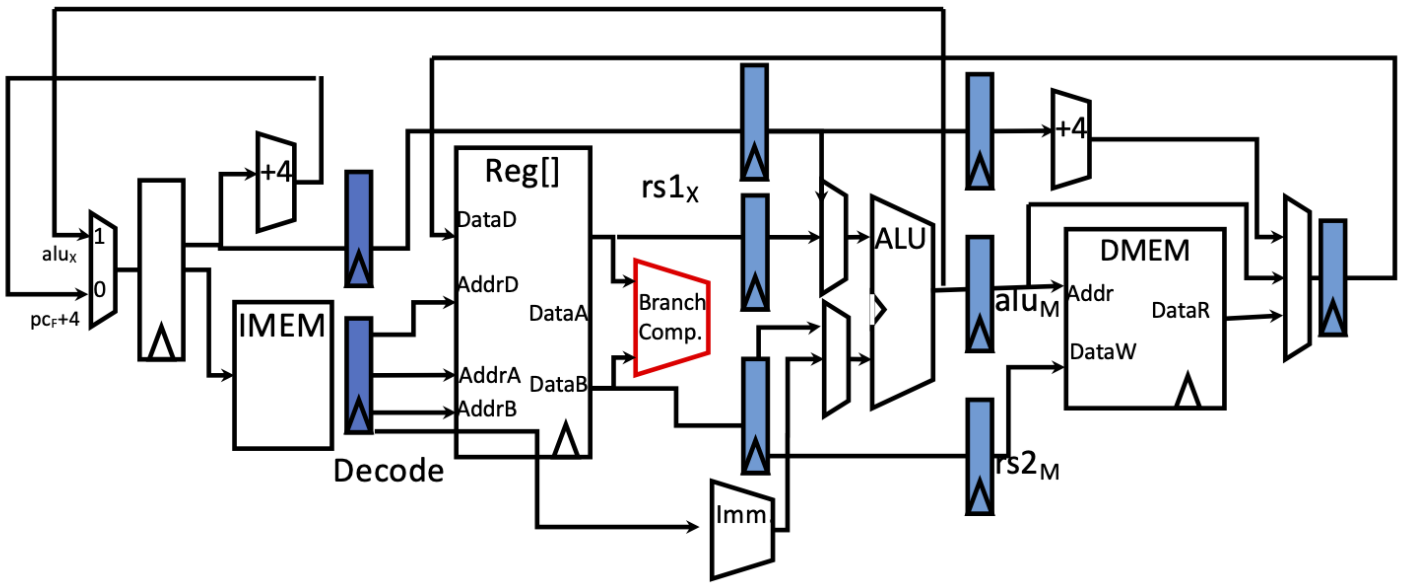
62. What is the instruction in IF stage of t = 7 (Part 3)?

[ ] 3: addi t1,t1,1
[ ] 4: beq a0,t1,choice1
[ ] 5: addi t1,t1,1
[ ] 6: beq a0,t1,choice2
[ ] 7: addi t1,t1,1
[ ] 8: beq a0,t1,choice3
[ ] 11: j end
[ ] 13: j end
[ ] 15: j end
[ ] 17: addi a0, zero, 10
[ ] 18: ecall

63. How many cycles does this program take to complete (Part 3)?

Part 4.

Now consider the pipeline modification below



- `The branch comparison has been moved to the decode stage`
- Note that branch addresses still get resolved only in the EX stage.
- Answer questions below. `Hint: Think about data hazards for the branch instruction`

Assume first instruction is addi a0,zero,2

64. What is the instruction in IF stage t = 6 ?

[ ] 2: addi a0,zero,2
[ ] 3: addi t1,t1,1
[ ] 4: beq a0,t1,choice1
[ ] 5: addi t1,t1,1
[ ] 6: beq a0,t1,choice2
[ ] 7: addi t1,t1,1
[ ] 8: beq a0,t1,choice3
[ ] 11: j end
[ ] 13: j end
[ ] 15: j end
[ ] 17: addi a0, zero, 10
[ ] 18: ecall

65. How many cycles does this program take to complete (Part 4) ?

F. Pipeline CPU. [4]

Consider the pipeline cpu above with the stage timings as shown below.

MUX	ALU	DMEM	Regfile	IMMGEN	BRANCH	IMEM
20	220	230	100	30	30	200

66. Assuming that this CPU is NOT Pipelined (i.e. it is a single cycle CPU), what is the shortest clock period possible to execute the instruction? _____

67. Assuming that this CPU is pipelined, what is the shortest clock period possible to execute the instruction? _____

dec	oct	hex	ch	dec	oct	hex	ch	dec	oct	hex	ch
32	40	20	(space)	64	100	40	@	96	140	60	`
33	41	21	!	65	101	41	A	97	141	61	a
34	42	22	"	66	102	42	B	98	142	62	b
35	43	23	#	67	103	43	C	99	143	63	c
36	44	24	$	68	104	44	D	100	144	64	d
37	45	25	%	69	105	45	E	101	145	65	e
38	46	26	&	70	106	46	F	102	146	66	f
39	47	27	'	71	107	47	G	103	147	67	g
40	50	28	(	72	110	48	H	104	150	68	h
41	51	29	)	73	111	49	I	105	151	69	i
42	52	2a	*	74	112	4a	J	106	152	6a	j
43	53	2b	+	75	113	4b	K	107	153	6b	k
44	54	2c	,	76	114	4c	L	108	154	6c	l
45	55	2d	-	77	115	4d	M	109	155	6d	m
46	56	2e	.	78	116	4e	N	110	156	6e	n
47	57	2f	/	79	117	4f	O	111	157	6f	o
48	60	30	0	80	120	50	P	112	160	70	p
49	61	31	1	81	121	51	Q	113	161	71	q
50	62	32	2	82	122	52	R	114	162	72	r
51	63	33	3	83	123	53	S	115	163	73	s
52	64	34	4	84	124	54	T	116	164	74	t
53	65	35	5	85	125	55	U	117	165	75	u
54	66	36	6	86	126	56	V	118	166	76	v
55	67	37	7	87	127	57	W	119	167	77	w
56	70	38	8	88	130	58	X	120	170	78	x
57	71	39	9	89	131	59	Y	121	171	79	y
58	72	3a	:	90	132	5a	Z	122	172	7a	z
59	73	3b	;	91	133	5b	[	123	173	7b	{
60	74	3c	<	92	134	5c	\	124	174	7c	|
61	75	3d	=	93	135	5d	]	125	175	7d	}
62	76	3e	>	94	136	5e	^	126	176	7e	~
63	77	3f	?	95	137	5f	_	127	177	7f	DEL (delete)