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Michael Pomper, for a photograph and biography, please see p. 238 of this issue.

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Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions

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***Abstract*—This paper considers the design, fabrication, and characterization of very small MOSFET switching devices suitable for digital integrated circuits using dimensions of the order of 1 μ. Scaling relationships are presented which show how a conventional MOSFET can be reduced in size. An improved small device structure is presented that uses ion implantation to provide shallow source and drain regions and a nonuniform substrate doping profile. One-dimensional models are used to predict the substrate doping profile and the corresponding threshold voltage versus source voltage characteristic. A two-dimensional current transport model is used to predict the relative degree of short-channel effects for different device parameter combinations. Polysilicon-gate MOSFET's with channel lengths as short as 0.5 μ were fabricated, and the device characteristics measured and compared with predicted values. The performance improvement expected from using these very small devices in highly miniaturized integrated circuits is projected.**

Manuscript received May 20, 1974; revised July 3, 1974.
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LIST OF SYMBOLS

α	Inverse semilogarithmic slope of subthreshold characteristic.
D	Width of idealized step function profile for channel implant.
ΔW_f	Work function difference between gate and substrate.
ϵ_{Si}, ϵ_{ox}	Dielectric constants for silicon and silicon dioxide.
I_d	Drain current.
k	Boltzmann's constant.
κ	Unitless scaling constant.
L	MOSFET channel length.
μ_{eff}	Effective surface mobility.
n_i	Intrinsic carrier concentration.
N_a	Substrate acceptor concentration.
Ψ_s	Band bending in silicon at the onset of strong inversion for zero substrate voltage.

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Ψ_b	Built-in junction potential.
q	Charge on the electron.
Q_{eff}	Effective oxide charge.
t_{ox}	Gate oxide thickness.
T	Absolute temperature.
V_d, V_s, V_g, V_{sub}	Drain, source, gate and substrate voltages.
V_{ds}	Drain voltage relative to source.
V_{s-sub}	Source voltage relative to substrate.
V_t	Gate threshold voltage.
w_s, w_d	Source and drain depletion layer widths.
W	MOSFET channel width.

Introduction

NEW HIGH resolution lithographic techniques for forming semiconductor integrated circuit patterns offer a decrease in linewidth of five to ten times over the optical contact masking approach which is commonly used in the semiconductor industry today. Of the new techniques, electron beam pattern writing has been widely used for experimental device fabrication [1]–[4] while X-ray lithography [5] and optical projection printing [6] have also exhibited high-resolution capability. Full realization of the benefits of these new high-resolution lithographic techniques requires the development of new device designs, technologies, and structures which can be optimized for very small dimensions.

This paper concerns the design, fabrication, and characterization of very small MOSFET switching devices suitable for digital integrated circuits using dimensions of the order of 1 μ. It is known that reducing the source-to-drain spacing (i.e., the channel length) of an FET leads to undesirable changes in the device characteristics. These changes become significant when the depletion regions surrounding the source and drain extend over a large portion of the region in the silicon substrate under the gate electrode. For switching applications, the most undesirable "short-channel" effect is a reduction in the gate threshold voltage at which the device turns on, which is aggravated by high drain voltages. It has been shown that these short-channel effects can be avoided by scaling down the vertical dimensions (e.g., gate insulator thickness, junction depth, etc.) along with the horizontal dimensions, while also proportionately decreasing the applied voltages and increasing the substrate doping concentration [7], [8]. Applying this scaling approach to a properly designed conventional-size MOSFET shows that a 200-Å gate insulator is required if the channel length is to be reduced to 1 μ.

A major consideration of this paper is to show how the use of ion implantation leads to an improved design for very small scaled-down MOSFET's. First, the ability of ion implantation to accurately introduce a low concentration of doping atoms allows the substrate doping profile in the channel region under the gate to be increased in a controlled manner. When combined with a relatively lightly doped starting substrate, this channel implant reduces the sensitivity of the threshold voltage to changes in the source-to-substrate ("backgate") bias. This reduced "substrate sensitivity" can then be traded off for a thicker gate insulator of 350-Å thickness which tends to be easier to fabricate reproducibly and reliably. Second, ion implantation allows the formation of very shallow source and drain regions which are more favorable with respect to short-channel effects, while maintaining an acceptable sheet resistance. The combination of these features in an all-implanted design gives a switching device which can be fabricated with a thicker gate insulator if desired, which has well-controlled threshold characteristics, and which has significantly reduced interelectrode capacitances (e.g., drain-to-gate or drain-to-substrate capacitances).

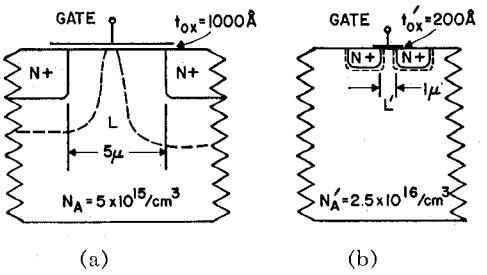

Fig. 1. Illustration of device scaling principles with $\kappa = 5$. (a) Conventional commercially available device structure. (b) Scaled-down device structure.

This paper begins by describing the scaling principles which are applied to a conventional MOSFET to obtain a very small device structure capable of improved performance. Experimental verification of the scaling approach is then presented. Next, the fabrication process for an improved scaled-down device structure using ion implantation is described. Design considerations for this all-implanted structure are based on two analytical tools: a simple one-dimensional model that predicts the substrate sensitivity for long channel-length devices, and a two-dimensional current-transport model that predicts the device turn-on characteristics as a function of channel length. The predicted results from both analyses are compared with experimental data. Using the two-dimensional simulation, the sensitivity of the design to various parameters is shown. Then, detailed attention is given to an alternate design, intended for zero substrate bias, which offers some advantages with respect to threshold control. Finally, the paper concludes with a discussion of the performance improvements to be expected from integrated circuits that use these very small FET's.

Device Scaling

The principles of device scaling [7], [8] show in a concise manner the general design trends to be followed in decreasing the size and increasing the performance of MOSFET switching devices. Fig. 1 compares a state-of-the-art n-channel MOSFET [9] with a scaled-down

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device designed following the device scaling principles to be described later. The larger structure shown in Fig. 1(a) is reasonably typical of commercially available devices fabricated by using conventional diffusion techniques. It uses a 1000-Å gate insulator thickness with a substrate doping and substrate bias chosen to give a gate threshold voltage V_t of approximately 2 V relative to the source potential. A substrate doping of 5×10^{15} cm^{-3} is low enough to give an acceptable value of substrate sensitivity. The substrate sensitivity is an important criterion in digital switching circuits employing source followers because the design becomes difficult if the threshold voltage increases by more than a factor of two over the full range of variation of the source voltage. For the device illustrated in Fig. 1(a), the design parameters limit the channel length L to about 5 μ. This restriction arises primarily from the penetration of the depletion region surrounding the drain into the area normally controlled by the gate electrode. For a maximum drain voltage of approximately 12–15 V this penetration will modify the surface potential and significantly lower the threshold voltage.

In order to design a new device suitable for smaller values of L, the device is scaled by a transformation in three variables: dimension, voltage, and doping. First, all linear dimensions are reduced by a unitless scaling factor κ, e.g., $t_{ox}' = t_{ox}/\kappa$, where the primed parameters refer to the new scaled-down device. This reduction includes vertical dimensions such as gate insulator thickness, junction depth, etc., as well as the horizontal dimensions of channel length and width. Second, the voltages applied to the device are reduced by the same factor (e.g., $V_{ds}' = V_{ds}/\kappa$). Third, the substrate doping concentration is increased, again using the same scaling factor (i.e., $N_a' = \kappa N_a$). The design shown in Fig. 1(b) was obtained using $\kappa = 5$ which corresponds to the desired reduction in channel length to 1 μ.

The scaling relationships were developed by observing that the depletion layer widths in the scaled-down device are reduced in proportion to the device dimensions due to the reduced potentials and the increased doping. For example,

$$w_s' = \{[2\epsilon_{Si}(\psi_b' + V_{s-sub}/\kappa)]/q\kappa N_a\}^{1/2} \simeq w_s/\kappa. \quad (1)$$

The threshold voltage at turn-on [9] is also decreased in direct proportion to the reduced device voltages so that the device will function properly in a circuit with reduced voltage levels. This is shown by the threshold voltage equation for the scaled-down device.

$$V_t' = (t_{ox}/\kappa\epsilon_{ox})\{-Q_{eff} + [2\epsilon_{Si}q\kappa N_a(\psi_s' + V_{s-sub}/\kappa)]^{1/2}\} + (\Delta W_f + \psi_s') \simeq V_t/\kappa. \quad (2)$$

In (2) the reduction in V_t is primarily due to the decreased insulator thickness, t_{ox}/κ, while the changes in the voltage and doping terms tend to cancel out. In most cases of interest (i.e., polysilicon gates of doping type opposite to that of the substrate or aluminum gates on p-type substrates) the work function difference ΔW_f is of opposite sign, and approximately cancels out ψ_s'. ψ_s' is the band bending in the silicon (i.e., the surface potential) at the onset of strong inversion for zero substrate bias. It would appear that the ψ' terms appearing in (1) and (2) prevent exact scaling since they remain approximately constant, actually increasing slightly due to the increased doping since $\psi_b' \simeq \psi_s' = (2kT/q) \ln (N_a'/n_i)$. However, the fixed substrate bias supply normally used with n-channel devices can be adjusted so that $(\psi_s' + V_{sub}') = (\psi_s + V_{sub})/\kappa$. Thus, by scaling down the applied substrate bias more than the other applied voltages, the potential drop across the source or drain junctions, or across the depletion region under the gate, can be reduced by κ.

All of the equations that describe the MOSFET device characteristics may be scaled as demonstrated above. For example, the MOSFET current equation [9] given by

$$I_d' = \frac{\mu_{eff}\epsilon_{ox}}{t_{ox}/\kappa}\left(\frac{W/\kappa}{L/\kappa}\right)\left(\frac{V_g - V_t - V_d/2}{\kappa}\right)(V_d/\kappa) = I_d/\kappa \quad (3)$$

is seen to be reduced by a factor of κ, for any given set of applied voltages, assuming no change in mobility. Actually, the mobility is reduced slightly due to increased impurity scattering in the heavier doped substrate.

It is possible to generalize the scaling approach to include electric field patterns and current density. The electric field distribution is maintained in the scaled-down device except for a change in scale for the spatial coordinates. Furthermore, the electric field strength at any corresponding point is unchanged because $V/x = V'/x'$. Thus, the carrier velocity at any point is also unchanged due to scaling and, hence, any saturation velocity effects will be similar in both devices, neglecting microscopic differences due to the fixed crystal lattice dimensions. From (3), since the device current is reduced by κ, the channel current per unit of channel width W is unchanged by scaling. This is consistent with the same sheet density of carriers (i.e., electrons per unit gate area) moving at the same velocity. In the vicinity of the drain, the carriers will move away from the surface to a lesser extent in the new device, due to the shallower diffusions. Thus, the density of mobile carriers per unit volume will be higher in the space-charge region around the drain, complementing the higher density of immobile charge due to the heavier doped substrate. Other scaling relationships for power density, delay time, etc., are given in Table I and will be discussed in a subsequent section on circuit performance.

In order to verify the scaling relationships, two sets of experimental devices were fabricated with gate insulators of 1000 and 200 Å (i.e., $\kappa = 5$). The measured drain voltage characteristics of these devices, normalized to $W/L = 1$, are shown in Fig. 2. The two sets of characteristics are quite similar when plotted with voltage and current scales of the smaller device reduced by a factor of five, which confirms the scaling predictions. In Fig. 2, the exact

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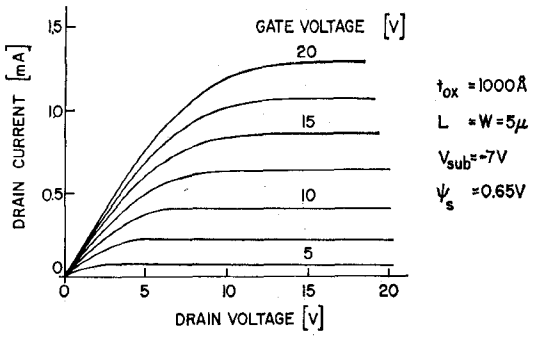
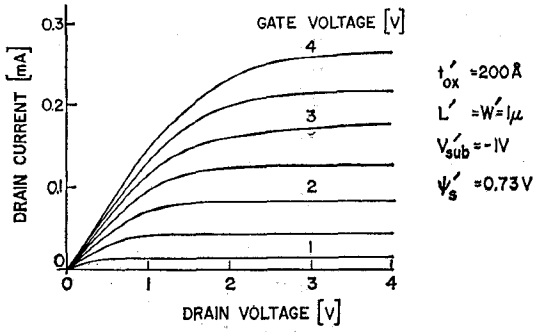


(a)



(b)

Fig. 2. Experimental drain voltage characteristics for (a) conventional, and (b) scaled-down structures shown in Fig. 1 normalized to $W/L = 1$.

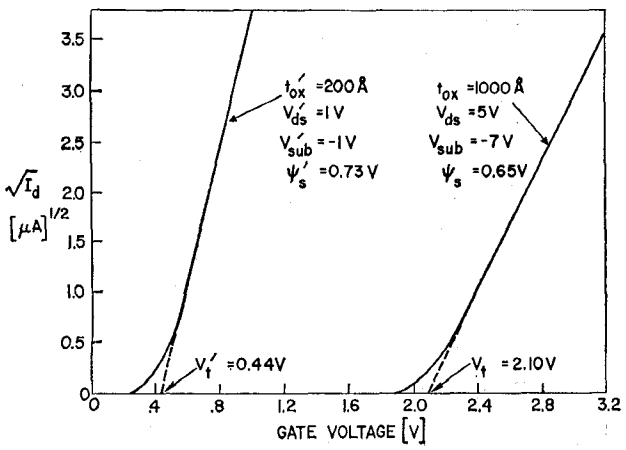


Fig. 3. Experimental turn-on characteristics for conventional and scaled-down devices shown in Fig. 1 normalized to $W/L = 1$.

match on the current scale is thought to be fortuitous since there is some experimental uncertainty in the magnitude of the channel length used to normalize the characteristics (see Appendix). More accurate data from devices with larger width and length dimensions on the same chip shows an approximate reduction of ten percent in mobility for devices with the heavier doped substrate. That the threshold voltage also scales correctly by a factor of five is verified in Fig. 3, which shows the experimental $\sqrt{I_d}$ versus V_g turn-on characteristics for the original and the scaled-down devices. For the cases shown, the drain voltage is large enough to cause pinchoff and the characteristics exhibit the expected linear relationship. When projected to intercept the gate voltage axis this linear relationship defines a threshold voltage useful for most logic circuit design purposes.

One area in which the device characteristics fail to scale is in the subthreshold or weak inversion region of the turn-on characteristic. Below threshold, I_d is exponentially dependent on V_g with an inverse semilogarithmic slope, α, [10], [11] which for the scaled-down device is given by

$$\alpha'\left(\frac{\text{volts}}{\text{decade}}\right) = \frac{dV_g'}{d\log_{10} I_d'}$$

$$= (kT/q \log_{10} e)\left(1 + \frac{\epsilon_{si} t_{ox}/\kappa}{\epsilon_{ox} w_d/\kappa}\right), \qquad (4)$$

which is the same as for the original larger device. The parameter α is important to dynamic memory circuits because it determines the gate voltage excursion required to go from the low current "off" state to the high current "on" state [11]. In an attempt to also extend the linear scaling relationships to α one could reduce the operating temperature in (4) (i.e., $T' = T/\kappa$), but this would cause a significant increase in the effective surface mobility [12] and thereby invalidate the current scaling relationship of (3). In order to design devices for operation at room temperature and above, one must accept the fact that the subthreshold behavior does not scale as desired. This nonscaling property of the subthreshold characteristic is of particular concern to miniature dynamic mem-

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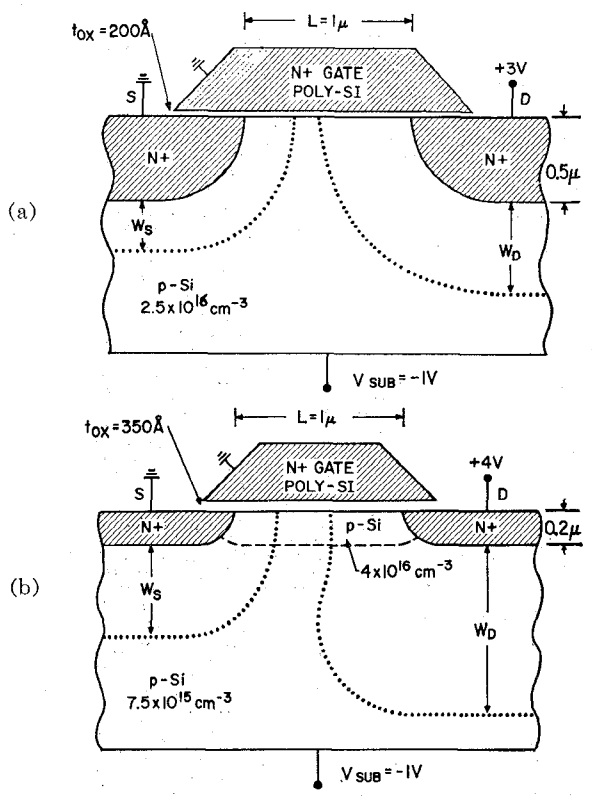

Fig. 4. Detailed cross sections for (a) scaled-down device structure, and (b) corresponding ion-implanted device structure.

ory circuits which require low source-to-drain leakage currents.

Ion-Implanted Device Design

The scaling considerations just presented lead to the device structure with a 1-μ channel length shown in Fig. 4(a). In contrast, the corresponding improved design utilizing the capability afforded by ion implantation is shown in Fig. 4(b). The ion-implanted device uses an initial substrate doping that is lower by about a factor of four, and an implanted boron surface layer having a concentration somewhat greater than the concentration used throughout the unimplanted structure of Fig. 4(a). The concentration and the depth of the implanted surface layer are chosen so that this heavier doped region will be completely within the surface depletion layer when the device is turned on with the source grounded. Thus, when the source is biased above ground potential, the depletion layer will extend deeper into the lighter doped substrate, and the additional exposed "bulk" charge will be reasonably small and will cause only a modest increase in the gate-to-source voltage required to turn on the device. With this improvement in substrate sensitivity the gate insulator thickness can be increased to as much as 350 Å and still maintain a reasonable gate threshold voltage as will be shown later.

Another aspect of the design philosophy is to use shallow implanted n^+ regions of depth comparable to the implanted p-type surface layer. The depletion regions under the gate electrode at the edges of the source and drain are then inhibited by the heavier doped surface layer, roughly pictured in Fig. 4(b), for the case of a turned-off device. The depletion regions under the source and drain extend much further into the lighter doped substrate. With deeper junctions these depletion regions would tend to merge in the lighter doped material which would cause a loss of threshold control or, in the extreme, punchthrough at high drain voltages. However, the shallower junctions give a more favorable electric field pattern which avoids these effects when the substrate doping concentration is properly chosen (i.e., when it is not too light).

The device capacitances are reduced with the ion-implanted structure due to the increased depletion layer width separating the source and drain from the substrate [cf. Figs. 4(a) and 4(b)], and due to the natural self-alignment afforded by the ion implantation process which reduces the overlap of the polysilicon gate over the source and drain regions. The thicker gate insulator also gives reduced gate capacitance, but the performance benefit in this respect is offset by the decreased gate field. To compensate for the thicker gate oxide and the expected threshold increase, a design objective for maximum drain voltage was set at 4 V for the ion-implanted design in Fig. 4(b), compared to 3 V for the scaled-down device of Fig. 4(a).

Fabrication of Ion-Implanted MOSFET's

The fabrication process for the ion-implanted MOSFET's used in this study will now be described. A four-mask process was used to fabricate polysilicon-gate, n-channel MOSFET's on a test chip which contains devices with channel lengths ranging from 0.5 to 10 μ. Though the eventual aim is to use electron-beam pattern exposure, it was more convenient to use contact masking with high quality master masks for process development. For this purpose high resolution is required only for the gate pattern which uses lines as small as 1.5 μ which are reduced in the subsequent processing. The starting substrate resistivity was 2 $\Omega\cdot$cm (i.e., about 7.5×10^{15} cm^{-3}). The method of fabrication for the thick oxide isolation between adjacent FET's is not described as it is not essential to the work presented here, and because several suitable techniques are available. Following dry thermal growth of the gate oxide, low energy (40 keV), low dose (6.7×10^{11} atoms/cm^2) B^{11} ions were implanted into the wafers, raising the boron doping near the silicon surface. All implantations were performed after gate oxide growth in order to restrict diffusion of the implanted regions.

After the channel implantation, a 3500-Å thick polysilicon layer was deposited, doped n^+, and the gate regions delineated. Next, n^+ source and drain regions 2000-Å deep were formed by a high energy (100 keV), high dose (4×10^{15} atoms/cm^2) As^{75} implantation through the same 350-Å oxide layer. During this step, however, the

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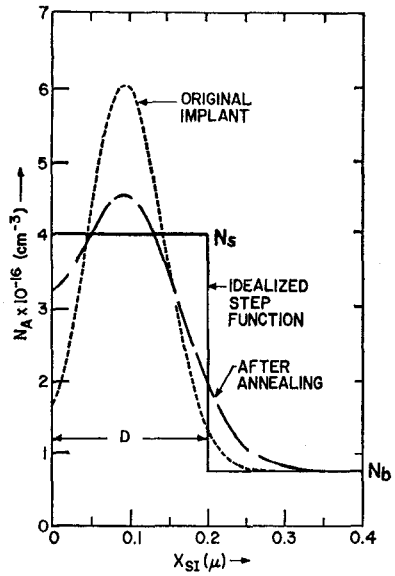

Fig. 5. Predicted substrate doping profile for basic ion-implanted device design for 40 keV B^{11} ions implanted through the 350-Å gate insulator.

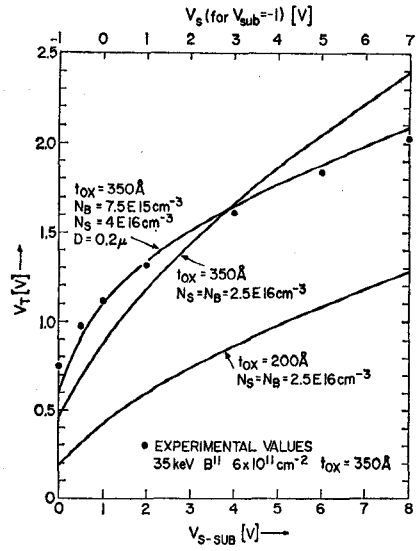

Fig. 6. Calculated and experimental substrate sensitivity characteristics for non-implanted devices with 200- and 350-Å gate insulators, and for corresponding ion-implanted device with 350-Å gate insulator.

polysilicon gate masks the channel region from the implant, absorbing all of the As^{75} dose incident there. The etching process used to delineate the gates results in a sloping sidewall which allows a slight penetration of As^{75} ions underneath the edges of the gates. The gate-to-drain (or source) overlap is estimated to be of the order of 0.2 μ. The high temperature processing steps that follow the implantations include 20 min at 900°C, and 11 min at 1000°C, which is more than adequate to anneal out the implantation damage without greatly spreading out the implanted doses. Typical sheet resistances were 50 Ω/□ for the source and drain regions, and 40 Ω/□ for the polysilicon areas. Following the As^{75} implant, a final insulating oxide layer 2000-Å thick was deposited using low-temperature chemical-vapor deposition. Then, the contact holes to the n^+ and polysilicon regions were defined, and the metalization was applied and delineated. Electrical contact directly to the shallow implanted source and drain regions was accomplished by a suitably chosen metallurgy to avoid junction penetration due to alloying during the final annealing step. After metalization an annealing step of 400 °C for 20 min in forming gas was performed to decrease the fast-state density.

One-Dimensional (Long Channel) Analysis

The substrate doping profile for the 40 keV, 6.7×10^{11} atoms/cm^2 channel implant incident on the 350-Å gate oxide, is shown in Fig. 5. Since the oxide absorbs 3 percent of the incident dose, the active dose in the silicon is 6.5×10^{11} atoms/cm^2. The concentration at the time of the implantation is given by the lightly dashed Gaussian function added to the background doping level, N_b. For 40 keV B^{11} ions, the projected range and standard deviation were taken as 1300 Å and 500 Å, respectively [13]. After the heat treatments of the subsequent processing, the boron is redistributed as shown by the heavier dashed line. These predicted profiles were obtained using a computer program developed by F. F. Morehead of our laboratories. The program assumes that boron atoms diffusing in the silicon reflect from the silicon-oxide interface and thereby raise the surface concentration. For modeling purposes it is convenient to use a simple, idealized, step-function representation of the doping profile, as shown by the solid line in Fig. 5. The step profile approximates the final predicted profile rather well and offers the advantage that it can be described by a few simple parameters. The three profiles shown in Fig. 5 all have the same active dose.

Using the step profile, a model for determining threshold voltage has been developed from piecewise solutions of Poisson's equation with appropriate boundary conditions [11]. The one-dimensional model considers only the vertical dimension and cannot account for horizontal short-channel effects. Results of the model are shown in Fig. 6 which plots the threshold voltage versus source-to-substrate bias for the ion-implanted step profile shown in Fig. 5. For comparison, Fig. 6 also shows the substrate sensitivity characteristics for the nonimplanted device with a 200-Å gate insulator and a constant background doping, and for a hypothetical device having a 350-Å gate insulator like the implanted structure and a constant background doping like the nonimplanted structure. The nonimplanted 200-Å case exhibits a low substrate sensitivity, but the magnitude of the threshold voltage is also low. On the other hand, the nonimplanted 350-Å case shows a higher threshold, but with an undesirably high substrate sensitivity. The ion-implanted case offers both a sufficiently high threshold voltage and a reasonably low substrate sensitivity, particularly for $V_{s\text{-sub}} \geq 1$ V. For $V_{s\text{-sub}} < 1$ V, a steep slope occurs because the

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surface inversion layer in the channel is obtained while the depletion region in the silicon under the gate does not exceed D, the step width of the heavier doped implanted region. For $V_{s\text{-sub}} \geq 1$ V, at inversion the depletion region now extends into the lighter doped substrate and the threshold voltage then increases relatively slowly with $V_{s\text{-sub}}$ [11]. Thus, with a fixed substrate bias of -1 V, the substrate sensitivity over the operating range of the source voltage (e.g., ground potential to 4 V) is reasonably low and very similar to the slope of the non-implanted 200-Å design. However, the threshold voltage is significantly higher for the implanted design which allows adequate design margin so that, under worst case conditions (e.g., short-channel effects which reduce the threshold considerably), the threshold will still be high enough so that the device can be turned off to a negligible conduction level as required for dynamic memory applications.

Experimental results are also given in Fig. 6 from measurements made on relatively long devices (i.e., $L = 10\ \mu$) which have no short-channel effects. These data agree reasonably well with the calculated curve. A 35 keV, 6×10^{11} atoms/cm^2 implant was used to achieve this result, rather than the slightly higher design value of 40 keV and 6.7×10^{11} atoms/cm^2.

Two-Dimensional (Short Channel) Analysis

For devices with sufficiently short-channel lengths, the one-dimensional model is inadequate to account for the threshold voltage lowering due to penetration of the drain field into the channel region normally controlled by the gate. While some models have been developed which account for this behavior [14], the problem is complicated for the ion-implanted structure by the non-uniform doping profile which leads to an electric field pattern that is difficult to approximate. For the ion-implanted case, the two-dimensional numerical current transport model of Kennedy and Mock [15], [16] was utilized. The computer program was modified by W. Chang and P. Hwang [17] to handle the abrupt substrate doping profiles considered for these devices.

The numerical current transport model was used to calculate the turn-on behavior of the ion-implanted device by a point-by-point computation of the device current for increasing values of gate voltage. Calculated results are shown in Fig. 7 for two values of channel length in the range of 1 μ, as well as for a relatively long-channel device with $L = 10\ \mu$. All cases were normalized to a width-to-length ratio of unity, and a drain voltage of 4 V was used in all cases. As the channel length is reduced to the order of 1 μ, the turn-on characteristic shifts to a lower gate voltage due to a lowering of the threshold voltage. The threshold voltage occurs at about 10^{-7} A where the turn-on characteristics make a transition from the exponential subthreshold behavior (a linear response on this semilogarithmic plot) to the $I_d \propto V_g^2$ square-law behavior. This current level can also be

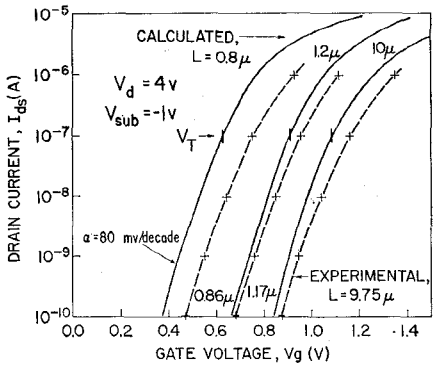

Fig. 7. Caluculated and experimental subthreshold turn-on characteristic for basic ion-implanted design for various channel lengths with $V_{\text{sub}} = -1$ V, $V_d = 4$ V.

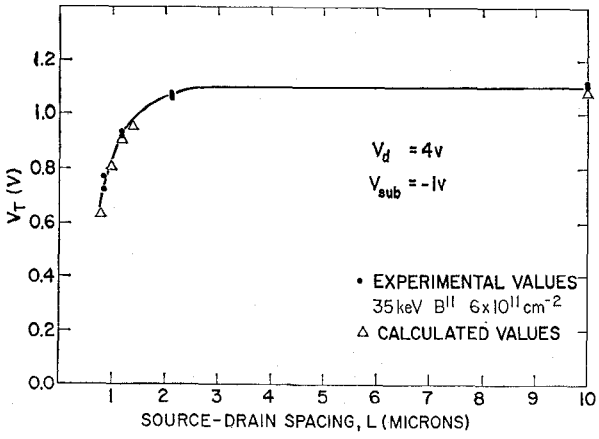

Fig. 8. Experimental and calculated dependence of threshold voltage on channel length for basic ion-implanted design with $V_{\text{sub}} = -1$ V, $V_d = 4$ V.

identified from Fig. 3 as the actual current at the projected threshold voltage, V_t. When the computed characteristics were plotted in the manner of Fig. 3 they gave 4×10^{-8} A at threshold for all device lengths. The band bending, ψ_s, at this threshold condition is approximately 0.75 V. Some of the other device designs considered with heavier substrate concentrations gave a higher current at threshold, so, for simplicity, the value of 10^{-7} A was used in all cases with a resultant small error in V_t.

MOSFET's with various channel lengths were measured to test the predictions of the two-dimensional model. The technique for experimentally determining the channel length for very short devices is described in the Appendix. The experimental results are plotted in Fig. 7 and show good agreement with the calculated curves, especially considering the somewhat different values of L. Another form of presentation of this data is shown in Fig. 8 where the threshold voltage is plotted as a function of channel length. The threshold voltage is essentially constant for $L > 2\ \mu$, and falls by a reasonably small amount as L is decreased from 2 to 1 μ, and then decreases more rapidly with further reductions in L. For

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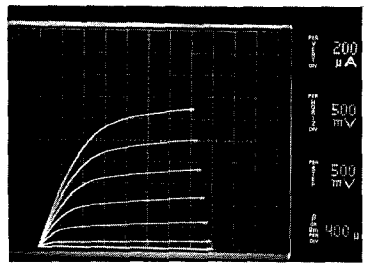

Fig. 9. Experimental drain voltage characteristics for basic ion-implanted design with $V_{sub} = -1$ V, $L = 1.1\ \mu$, and $W = 12.2\ \mu$. Curve tracer parameters; load resistance 30 Ω, drain voltage 4 V, gate voltage 0–4 V in 8 steps each 0.5 V apart.

circuit applications the nominal value of L could be set somewhat greater than 1 μ so that, over an expected range of deviation of L, the threshold voltage is reasonably well controlled. For example, $L = 1.3 \pm 0.3\ \mu$ would give $V_t = 1.0 \pm 0.1$ V from chip to chip due to this short-channel effect alone. This would be tolerable for many circuit applications because of the tracking of different devices on a given chip, if indeed this degree of control of L can be achieved. The experimental drain characteristics for an ion-implanted MOSFET with a 1.1-μ channel length are shown in Fig. 9 for the grounded source condition. The general shape of the characteristics is the same as those observed for much larger devices. No extraneous short-channel effects were observed for drain voltages as large as 4 V. The experimental data in Figs. 6–9 were taken from devices using a B^{11} channel implantation energy and dose of 35 keV and 6.0×10^{11} atoms/cm^2, respectively.

The two-dimensional simulations were also used to test the sensitivity of the design to various parameters. The results are given in Fig. 10 which tabulates values of threshold voltage as a function of channel length for the indicated voltages. Fig. 10(a) is an idealized representation for the basic design that has been discussed thus far. The first perturbation to the basic design was an increase in junction depth to 0.4 μ. This was found to give an appreciable reduction in threshold voltage for the shorter devices in Fig. 10(b). Viewed another way, the minimum device length would have to be increased by 20 percent (from 1.0 to 1.2 μ) to obtain a threshold comparable to the basic design. This puts the value of the shallower junctions in perspective. Another perturbation from the basic design which was considered was the use of a substrate doping lighter by a factor of 2, with a slightly higher concentration in the surface layer to give the same threshold for a long-channel device [Fig. 10(c)]. The results for smaller devices proved to be similar to the case of deeper junctions. The next possible departure from the basic design is the use of a shallower boron implantation in the channel region, only half as deep, with a heavier concentration to give the same long-channel threshold [Fig. 10(d)]. With the shallower profile, and

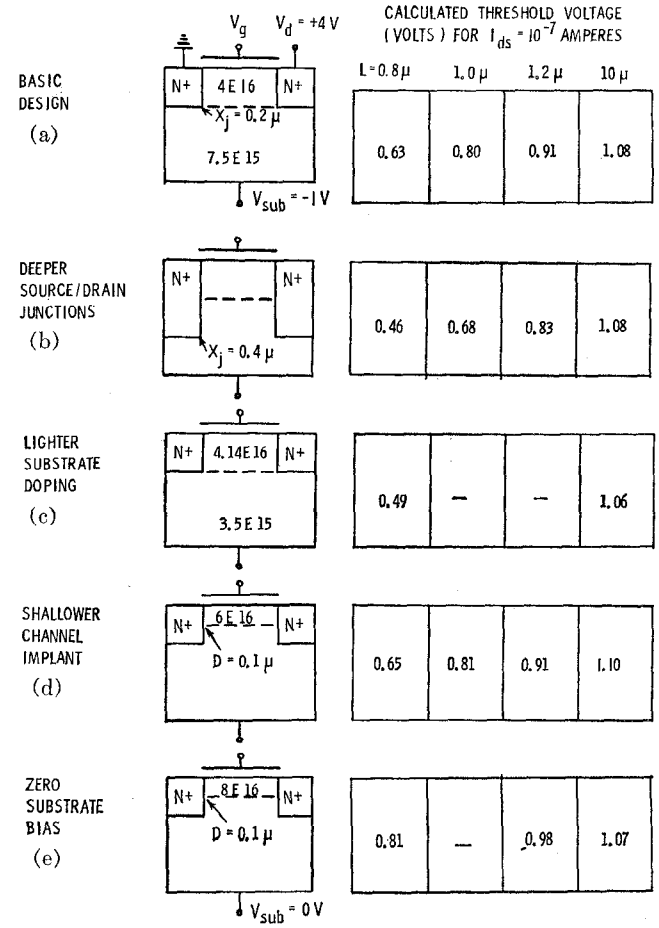

Fig. 10. Threshold voltage calculated using two-dimensional current transport model for various parameter conditions. A flat-band voltage of —1.1 V is assumed.

considering that the boron dose implanted in the silicon is about 20 percent less in this case, it was expected that more short-channel effects would occur. However, the calculated values show almost identical thresholds compared to the basic design. With the shallower implantation it is possible to use zero substrate bias and still have good substrate sensitivity since the heavier doped region is completely depleted at turn-on with a grounded source. The last design perturbation considers such a case, again with a heavier concentration to give the same long-channel threshold [Fig. 10 (e)]. The calculations for this case show appreciably less short-channel effect. In fact, the threshold for this case for a device with $L = 0.8\ \mu$ is about the same as for an $L = 1.0\ \mu$ device of the basic design. This important improvement is apparently due to the reduced depletion layer widths around the source and drain with the lower voltage drop across those junctions. Also, with these bias and doping conditions, the depletion layer depth in the silicon under the gate is much less at threshold, particularly near the source where only the band bending, ψ_s, appears across this depletion region, which may help prevent the penetration of field lines from the drain into this region where the device turn-on is controlled.

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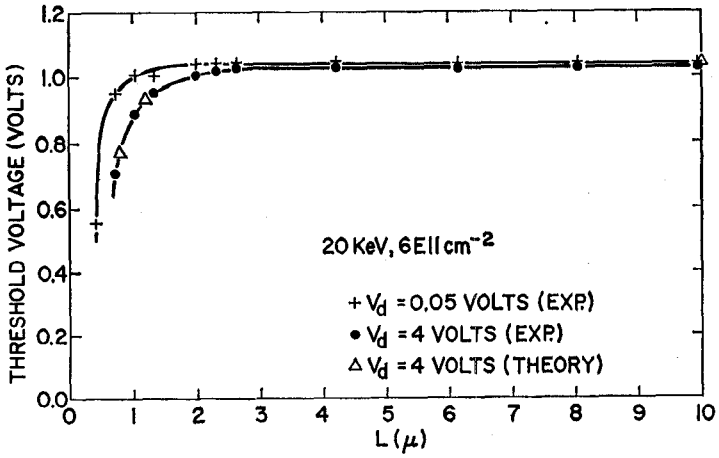

Fig. 11. Experimental and calculated dependence of threshold voltage on channel length for ion-implanted zero substrate bias design.

Characteristics of the Zero Substrate Bias Design

Since the last design shown in Fig. 10(e) appears to be better behaved in terms of short-channel effects, it is worthwhile to review its properties more fully. Experimental devices corresponding to this design were built and tested with various channel lengths. In this case a 20 keV, 6.0×10^{11} atoms/cm^2 B^{11} implant was used to obtain a shallower implanted layer of approximately 1000-Å depth [11]. Data on threshold voltage for these devices with 4 V applied to the drain is presented in Fig. 11 and corresponds very well to the calculated values. Data for a small drain voltage is also given in this figure, showing much less variation of threshold with channel length, as expected. The dependence of threshold voltage on source-to-substrate bias is shown in Fig. 12 for different values of L. The drain-to-source voltage was held at a constant low value for this measurement. The results show that the substrate sensitivity is indeed about the same for this design with zero substrate bias as for the original design with $V_{sub} = -1$ V. Note that the smaller devices show a somewhat flatter substrate sensitivity characteristic with relatively lower thresholds at high values of source (and drain) voltage.

The turn-on characteristics for the zero substrate bias design, both experimental and calculated, are shown in Fig. 13 for different values of L. The relatively small shift in threshold for the short-channel devices is evident; however, the turn-on rate is considerably slower for this case than for the $V_{sub} = -1$ V case shown in Fig. 7. This is due to the fact that the depletion region in the silicon under the gate is very shallow for this zero substrate bias case so that a large portion of a given gate voltage change is dropped across the gate insulator capacitance rather than across the silicon depletion layer capacitance. This is discussed in some detail for these devices in another paper [11]. The consequence for dynamic memory applications is that, even though the zero substrate bias

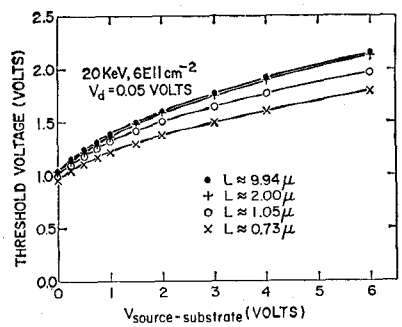

Fig. 12. Substrate sensitivity characteristics for ion-implanted zero substrate bias design with channel length as parameter.

design offers improved threshold control for strong inversion, this advantage is offset by the flatter subthreshold turn-on characteristic. For such applications the noise margin with the turn-on characteristic of Fig. 13 is barely suitable if the device is turned off by bringing its gate to ground. Furthermore, elevated temperature aggravates the situation [18]. Thus, for dynamic memory, the basic design with $V_{sub} = -1$ V presented earlier is preferred.

Circuit Performance with Scaled-Down Devices

The performance improvement expected from using very small MOSFET's in integrated circuits of comparably small dimensions is discussed in this section. First, the performance changes due to size reduction alone are obtained from the scaling considerations given earlier. The influence on the circuit performance due to the structural changes of the ion-implanted design is then discussed.

Table I lists the changes in integrated circuit performance which follow from scaling the circuit dimensions, voltages, and substrate doping in the same manner as the device changes described with respect to Fig. 1. These changes are indicated in terms of the dimensionless scal-

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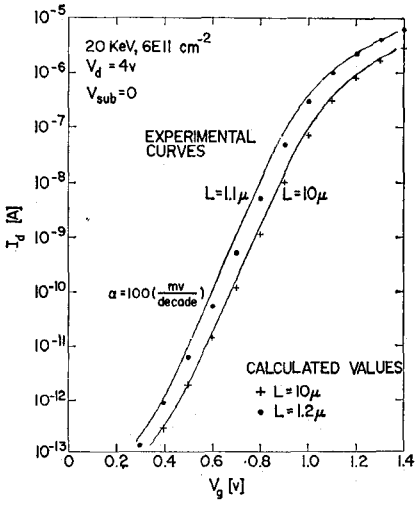

Fig. 13. Calculated and experimental subthreshold turn-on characteristics for ion-implanted zero substrate bias design.

TABLE I

SCALING RESULTS FOR CIRCUIT PERFORMANCE

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

ing factor κ. Justifying these results here in great detail would be tedious, so only a simplified treatment is given. It is argued that all nodal voltages are reduced in the miniaturized circuits in proportion to the reduced supply voltages. This follows because the quiescent voltage levels in digital MOSFET circuits are either the supply levels or some intermediate level given by a voltage divider consisting of two or more devices, and because the resistance V/I of each device is unchanged by scaling. An assumption is made that parasitic resistance elements are either negligible or unchanged by scaling, which will be examined subsequently. The circuits operate properly at lower voltages because the device threshold voltage V_t scales as shown in (2), and furthermore because the tolerance spreads on V_t should be proportionately reduced as well if each parameter in (2) is controlled to the same percentage accuracy. Noise margins are reduced, but at the same time internally generated noise coupling voltages are reduced by the lower signal voltage swings.

Due to the reduction in dimensions, all circuit elements (i.e., interconnection lines as well as devices) will have their capacitances reduced by a factor of κ. This occurs because of the reduction by κ^2 in the area of these components, which is partially cancelled by the decrease in the electrode spacing by κ due to thinner insulating films

TABLE II

SCALING RESULTS FOR INTERCONNECTION LINES

Parameter	Scaling Factor
Line resistance, $R_L = \rho L/Wt$	κ
Normalized voltage drop IR_L/V	κ
Line response time R_LC	1
Line current density I/A	κ

and reduced depletion layer widths. These reduced capacitances are driven by the unchanged device resistances V/I giving decreased transition times with a resultant reduction in the delay time of each circuit by a factor of κ. The power dissipation of each circuit is reduced by κ^2 due to the reduced voltage and current levels, so the power-delay product is improved by κ^3. Since the area of a given device or circuit is also reduced by κ^2, the power density remains constant. Thus, even if many more circuits are placed on a given integrated circuit chip, the cooling problem is essentially unchanged.

As indicated in Table II, a number of problems arise from the fact that the cross-sectional area of conductors is decreased by κ^2 while the length is decreased only by κ. It is assumed here that the thicknesses of the conductors are necessarily reduced along with the widths because of the more stringent resolution requirements (e.g., on etching, etc.). The conductivity is considered to remain constant which is reasonable for metal films down to very small dimensions (until the mean free path becomes comparable to the thickness), and is also reasonable for degenerately doped semiconducting lines where solid solubility and impurity scattering considerations limit any increase in conductivity. Under these assumptions the resistance of a given line increases directly with the scaling factor κ. The IR drop in such a line is therefore constant (with the decreased current levels), but is κ times greater in comparison to the lower operating voltages. The response time of an unterminated transmission line is characteristically limited by its time constant R_LC, which is unchanged by scaling; however, this makes it difficult to take advantage of the higher switching speeds inherent in the scaled-down devices when signal propagation over long lines is involved. Also, the current density in a scaled-down conductor is increased by κ, which causes a reliability concern. In conventional MOSFET circuits, these conductivity problems are relatively minor, but they become significant for linewidths of micron dimensions. The problems may be circumvented in high performance circuits by widening the power buses and by avoiding the use of n^+ doped lines for signal propagation.

Use of the ion-implanted devices considered in this paper will give similar performance improvement to that of the scaled-down device with $\kappa = 5$ given in Table I. For the implanted devices with the higher operating voltages (4 V instead of 3 V) and higher threshold voltages (0.9 V instead of 0.4 V), the current level will be reduced

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in proportion to $(V_g - V_t)^2/t_{ox}$ to about 80 percent of the current in the scaled-down device. The power dissipation per circuit is thus about the same in both cases. All device capacitances are about a factor of two less in the implanted devices, and n^+ interconnection lines will show the same improvement due to the lighter substrate doping and decreased junction depth. Some capacitance elements such as metal interconnection lines would be essentially unchanged so that the overall capacitance improvement in a typical circuit would be somewhat less than a factor of two. The delay time per circuit which is proportional to VC/I thus appears to be about the same for the implanted and for the directly scaled-down micron devices shown in Fig. 4.

Summary

This paper has considered the design, fabrication, and characterization of very small MOSFET switching devices. These considerations are applicable to highly miniaturized integrated circuits fabricated by high-resolution lithographic techniques such as electron-beam pattern writing. A consistent set of scaling relationships were presented that show how a conventional device can be reduced in size; however, this direct scaling approach leads to some challenging technological requirements such as very thin gate insulators. It was then shown how an all ion-implanted structure can be used to overcome these difficulties without sacrificing device area or performance. A two-dimensional current transport model modified for use with ion-implanted structures proved particularly valuable in predicting the relative degree of short-channel effects arising from different device parameter combinations. The general objective of the study was to design an n-channel polysilicon-gate MOSFET with a 1-μ channel length for high-density source-follower circuits such as those used in dynamic memories. The most satisfactory combination of subthreshold turn-on range, threshold control, and substrate sensitivity was achieved by an experimental MOSFET that used a 35 keV, 6.0×10^{11} atoms/cm^2 B^{11} channel implant, a 100 keV, 4×10^{15} atoms/cm^2 As^{75} source/drain implant, a 350-Å gate insulator, and an applied substrate bias of -1 V. Also presented was an ion-implanted design intended for zero substrate bias that is more attractive from the point of view of threshold control but suffers from an increased subthreshold turn-on range. Finally the sizable performance improvement expected from using very small MOSFET's in integrated circuits of comparably small dimensions was projected.

Appendix

Experimental Determination of Channel Length

A technique for determining the effective electrical channel length L for very small MOSFET's from experimental data is described here. The technique is based on the observation that

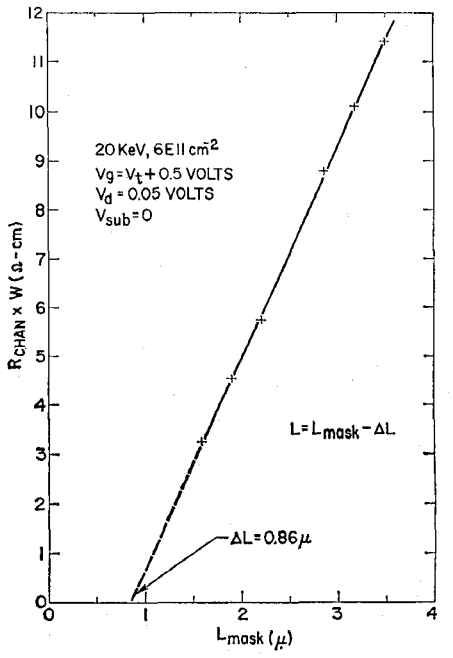

Fig. 14. Illustration of experimental technique used to determine channel length, L.

$$WR_{\text{chan}} = L\rho_{\text{chan}} \tag{A1}$$

where R_{chan} is the channel resistance, and ρ_{chan} the sheet resistance of the channel. For a fixed value of $V_g - V_t > 0$, and with the device turned on in the below-pinchoff region, the channel sheet resistance is relatively independent of L. Then, a plot of WR_{chan} versus L_{mask} will intercept the L_{mask} axis at ΔL because $\Delta L = L_{\text{mask}} - L$, where ΔL is the processing reduction in the mask dimension due to exposure and etching. An example of this technique is illustrated in Fig. 14.

The experimental values of W and R_{chan} used in Fig. 14 were obtained as follows. First, the sheet resistance of the ion-implanted n^+ region was determined using a relatively large four-point probe structure. Knowing the n^+ sheet resistance allows us to compute the source and drain resistance R_s and R_d, and to deduce W from the resistance of a long, slender, n^+ line. The channel resistance can be calculated from

$$R_{\text{chan}} = V_{\text{chan}}/I_d = (V_d - I_d(R_s + R_d + 2R_c + R_{\text{load}}))/I_d, \tag{A2}$$

where R_c is the contact resistance of the source or drain, and R_{load} is the load resistance of the measurement circuit. I_d was determined at $V_g = V_t + 0.5$ V with a small applied drain voltage of 50 or 100 mV. The procedure is more simple and accurate if one uses a set of MOSFET's having different values of L_{mask} but all with the same value of W_{mask}. Then one needs only to plot R_{chan} versus L_{mask} in order to determine ΔL.

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ACKNOWLEDGMENT

We wish to acknowledge the valuable contributions of B. L. Crowder and F. F. Morehead who provided the ion implantations and related design information. Also important were the contributions of P. Hwang and W. Chang to two-dimensional device computations. J. J. Walker and V. DiLonardo assisted with the mask preparation and testing activities. The devices were fabricated by the staff of the silicon technology facility at the T. J. Watson Research Center.

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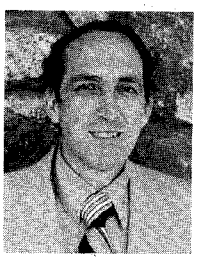
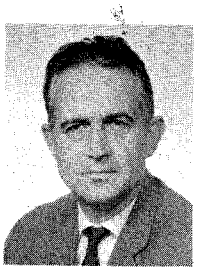


Robert H. Dennard (M'65) was born in Terrell, Tex., in 1932. He received the B.S. and M.S. degrees in electrical engineering from Southern Methodist University, Dallas, Tex., in 1954 and 1956, respectively, and the Ph.D. degree from Carnegie Institute of Technology, Pittsburgh, Pa., in 1958.

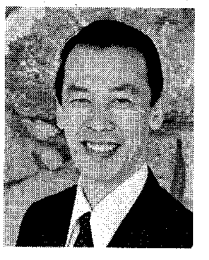
In 1958 he joined the IBM Research Division where his experience included study of new devices and circuits for logic and memory applications, and development of advanced data communication techniques. Since 1963 he has been at the IBM T. J. Watson Research Center, Yorktown Heights, N.Y., where he worked with a group exploring large-scale integration (LSI), while making contributions in cost and yield models, MOSFET device and integrated circuit design, and FET memory cells and organizations. Since 1971 he has been manager of a group which is exploring high density digital integrated circuits using advanced technology concepts such as electron beam pattern exposure.



Fritz H. Gaensslen was born in Tuebingen, Germany, on October 4, 1931. He received the Dipl. Ing and Dr. Ing. degrees in electrical engineering from the Technical University of Munich, Munich, Germany, in 1959 and 1966, respectively.

Prior to 1966 he served as Assistant Professor in the Department of Electrical Engineering, Technical University of Munich, Munich, Germany. During this period he was working on the synthesis of linear and digital networks. In 1966 he joined the IBM T. J. Watson Research Center, Yorktown Heights, N.Y., where he is currently a member of a semiconductor device and process design group. His current technical interests involve various aspects of advanced integrated circuits like miniaturization, device simulation, and ion implantation. From September 1973 he was on a one year assignment at the IBM Laboratory, Böeblingen, Germany.

Dr. Gaensslen is a member of the Nachrichtentechnische Gesellschaft.



Hwa-Nien Yu (M'65) was born in Shanghai, China, on January 17, 1929. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana, in 1953, 1954, and 1958, respectively.

While at the University, he was a Research Assistant in the Digital Computer Laboratory and worked on the design of the Illiac-II computer. Since joining the IBM Research Laboratory in 1957, he has been engaged in various exploratory solid-state device research activities. After working with the Advanced Systems Development Division from 1959 to 1962, he rejoined the Research Division in 1962 to work on the ultra-high speed germenium device technology. Since 1967, he has been engaged in advanced silicon LSI device technology research. He is currently the Manager of Semiconductor Technology at the IBM T. J. Watson Research Center, Yorktown Heights, N.Y.

Dr. Yu is a member of Sigma Xi.

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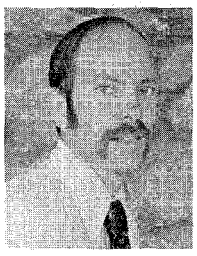

V. Leo Rideout (S'61–M'65) was born in N.J. in 1941. He received the B.S.E.E. degree with honors in 1963 from the University of Wisconsin, Madison, the M.S.E.E. degree in 1964 from Stanford University, Stanford, Calif., and the Ph.D. degree in materials science in 1970 from the University of Southern California (U.S.C.), Los Angeles. His thesis work at U.S.C. under Prof. C. R. Crowell concerned thermally assisted current transport in platinum silicide Schottky barriers.

From 1963 to 1965 he was a member of the technical staff of Bell Telephone Laboratories where he worked on high-frequency germanium transistors and metal-semiconductor Schottky barriers on potassium tantalate. In 1966 he spent a year as a Research Assistant in the department of Materials Science at the Technological University of Eindhoven, Eindhoven, The Netherlands, studying acoustoelectric effects in cadmium sulphide. In 1970 he joined IBM Research in the device research group of Dr. L. Esaki where he worked on fabrication and contact technology for multiheterojunction "superlattice" structures using gallium-arsenide-phosphide and gallium-aluminum-arsenide. Since 1972 he has been a member of the semiconductor device and circuit design group of Dr. R. Dennard at the IBM T. J. Watson Research Center, Yorktown Heights, N.Y. His present research interests concern high density silicon FET technology. He is the author or co-author of 20 technical papers and 3 U.S. Patents.

Dr. Rideout is a member of the Electrochemical Society, Tau Beta Pi, Eta Kappa Nu, Phi Kappa Phi, and Sigma Xi.

Ernest Bassous was born in Alexandria, Egypt, on September 1, 1931. He received the B.Sc. degree in chemistry from the University of London, London, England in 1953, and the M.S. degree in physical chemistry from the Polytechnic Institute of Brooklyn, Brooklyn, N.Y. in 1965.

From 1954 to 1959 he taught Chemistry and Physics at the British Boys' School, Alexandria, Egypt. He went to France in 1959 where he worked for 1 year on infra red detectors at the Centre National d'Etudes des Telecommunications, Issy-les-Moulineaux, Seine. From 1960 to 1964 he worked at the Thomas A. Edison Research Laboratory in West Orange, N.J., where his activities included studies in arc discharge phenomena, ultra violet absorption spectroscopy, and organic semiconductors. In 1964 he joined the IBM Research Laboratory, Yorktown Heights, N.Y., to work on semiconductors. As a member of the Research staff he is presently engaged in the study of materials and processes used in the fabrication of silicon integrated circuits.

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Andre R. LeBlanc (M'74) received the B.S. degree in electrical engineering, and the M.S. degree in physics from the University of Vermont, Burlington, in 1956 and 1959, respectively, and the D.Sc. degree in electrical engineering from the University of New Mexico, Albuquerque, in 1962.

Prior to joining IBM, Essex Junction, Vt., in 1957, he was affiliated with G.E. as an electrical engineer and also with Sandia Corporation in conjunction with the University of New Mexico. In 1959 he took an educational leave of absence to complete his doctorate. He is presently a member of the Exploratory Memory Group at the IBM Laboratory, Essex Junction, where his current technical interest includes a study of short-channel MOSFET devices. He has authored five publications and twelve papers, as well as several IBM Technical Reports.

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