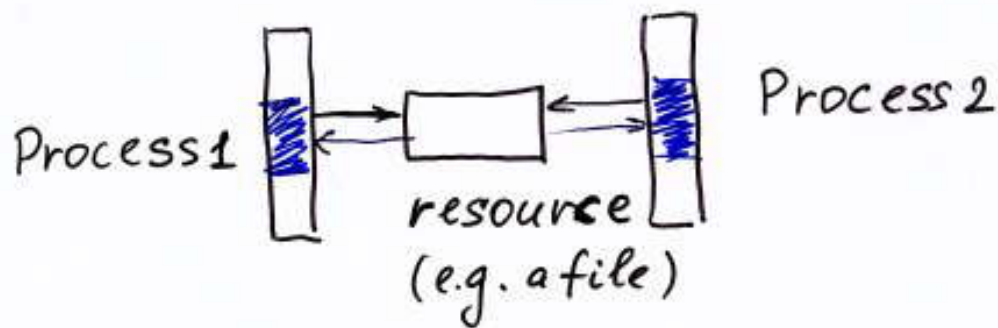


Mutual Exclusion



Critical sections of code
include all the access to the
shared resource

(only one process can be in its critical
section at a time)

Task: find a protocol for determining
which process is allowed
to enter its critical section
at which time

The protocol must have
the following properties :

Safety: only one process is
in its critical section at a time

Problem: a protocol, where none of the processes
ever enters its critical section is safe!
also, need:

Liveness: Whenever any process
wants to enter its critical section,
it will eventually be permitted to do so

non-blocking: A process can always
request to enter its critical section
(when in non-critical one)

no strict sequencing: Processes
need not enter their
critical section in strict sequence

(access of Process 1 and access of Process 2
to their critical sections don't have
to alternate.)



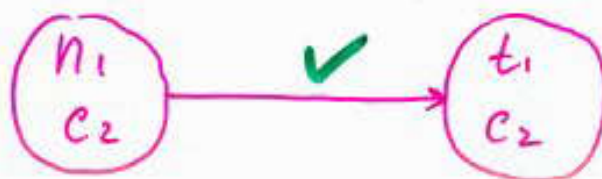
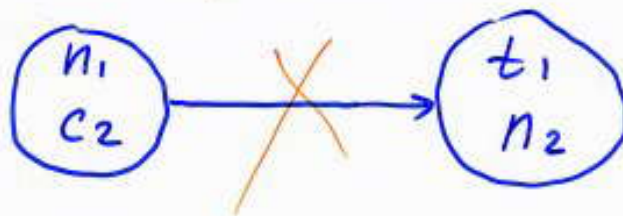
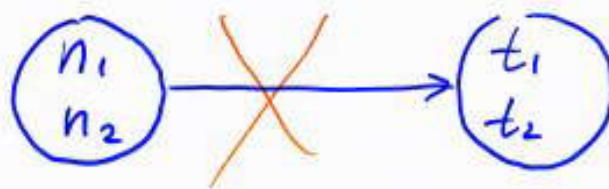
n_i process i is in its non-critical state

t_i process i is trying to enter its critical state

c_i process i is in its critical state

$n_i \rightarrow t_i \rightarrow c_i \rightarrow n_i \rightarrow t_i \rightarrow c_i \rightarrow n_i \dots$

only one process can make a transition (say, from n to t) at a time



not
allowed

allowed

LTL

Safety

$$G \neg (c_1 \wedge c_2)$$

Liveness

$$G(t_1 \rightarrow Fc_1)$$

$$G(t_2 \rightarrow Fc_2)$$

Non-blocking

—

CTL

$$AG \neg (c_1 \wedge c_2)$$

$$AG(t_1 \rightarrow AFc_1)$$

$$AG(t_2 \rightarrow AFc_2)$$

$$AG(t_1 \rightarrow EX \cdot)$$

$$AG(t_2 \rightarrow EXt_2)$$

Safety : ✓

For the first modelling attempt:

Liveness: ✗ because

there is a path, where t_1 is true in a state, but from that state on C_1 is false.

$S_0 \rightarrow S_1 \rightarrow S_3 \rightarrow S_7 \rightarrow S_1 \rightarrow S_3 \rightarrow S_7 \rightarrow \dots$
 loop loop

(similar for the second process)

non-blocking : ✓

for every state sat. n_1 , there is a successor sat. t_1

(similar for the second process)

No strict sequencing : ✓

there is a path where

$\dots \underbrace{C_2 C_2 C_2}_{C_2} \underbrace{C_1 C_1 C_1 \dots C_1}_{C_1} \underbrace{C_2 C_2 C_2}_{C_2} \underbrace{C_1 C_1}_{C_1} \underbrace{C_2 C_2 \dots C_2}_{C_2}$

such alternation does not occur (for each process)