The Past, Present and Future of Indexing on Persistent Memory

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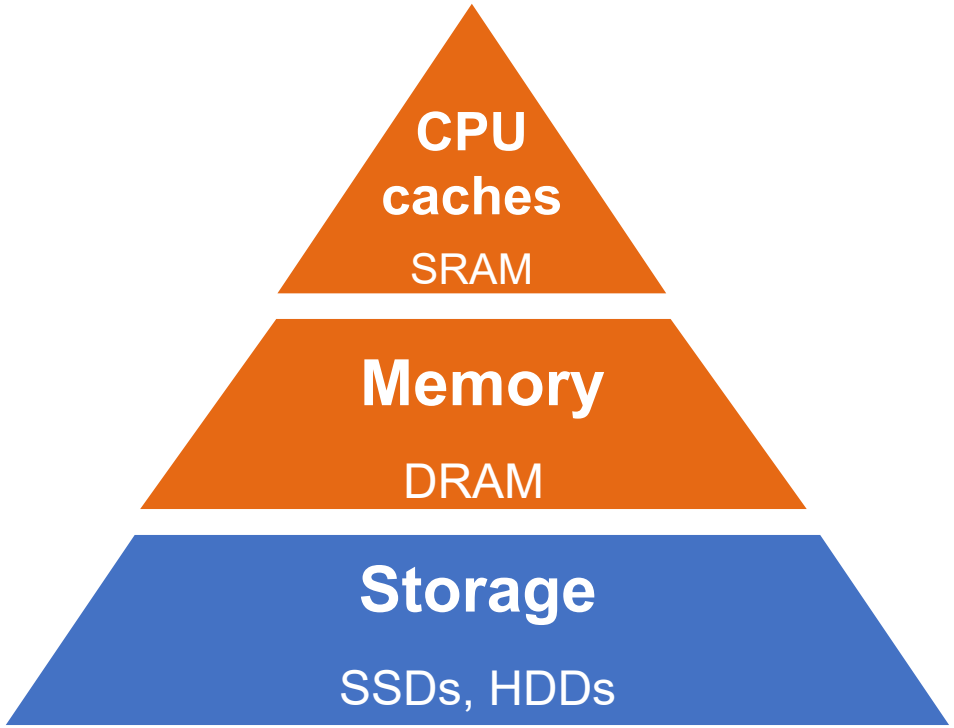
Outline

- Part 1 - The memory/storage landscape
  - Why new memory technologies?
  - Persistent memory hardware/software
- Part 2 - Range indexes
- Part 3 - Hash tables
- Part 4 - Implications and outlook
  - Especially, life after Optane

Part 1: PM and Storage Landscape

The (Traditional) Storage Hierarchy



Layers with clear boundaries

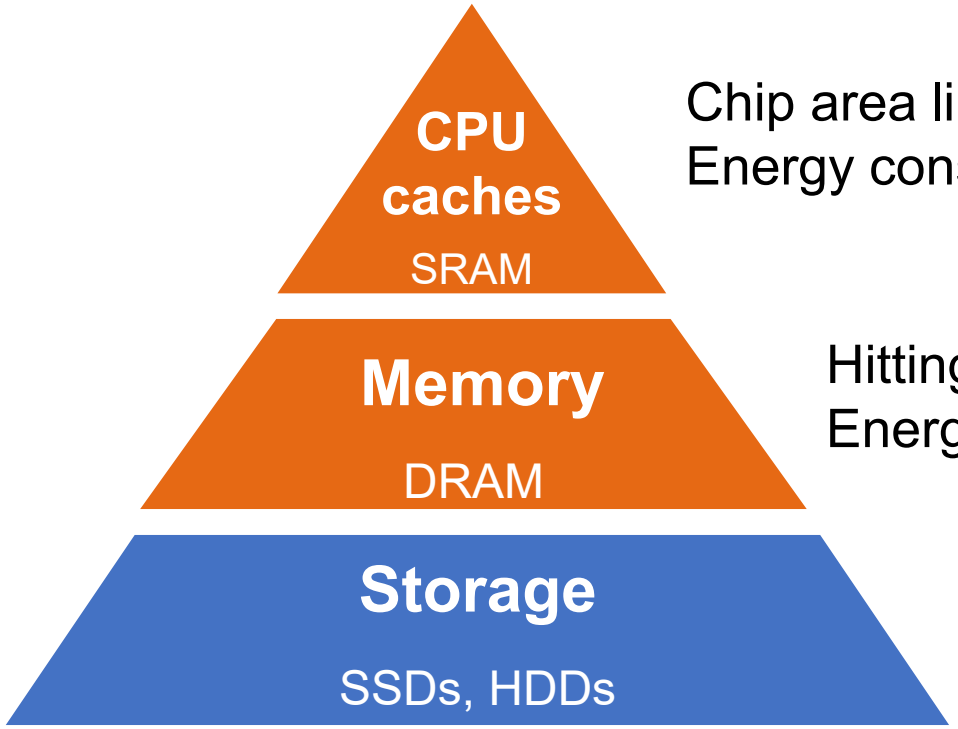
- Memory: fast but volatile
- Storage: slower than memory but persistent

Caching stores hugely successful

- Hot (index) pages in buffer pool (DRAM)
- Persist to SSDs
- Cost-effective

Facing several major challenges

Issues with in (Traditional) Storage Hierarchy



Chip area limits
Energy consumption

Hitting scalability limits (the “scaling wall”) [1]
Energy consumption

High access latency

Need new storage/memory media – mainly for ***better scalability/higher capacity + save energy***

Emerging Memory Techniques to the Rescue

- Phase change memory (PCM) [8]
  - Including Intel's 3D XPoint/Optane
  - Micron (with Intel and initially pre 2015)
- Spin-Transfer Torque Magnetic RAM (STT-RAM) [5]
  - Everspin
- Memristor [2]
  - Notable attempt by HP(E)'s The Machine [3, 4]
- Carbon NanoTube RAM (NRAM, NanoRAM) [6]
  - Nantero
- Ferroelectric RAM (FeRAM) [7]
  - Fujitsu

They just all happen to be non-volatile!

- *Various new flash/DRAM technologies – more on this later*

Persistent Memory

Aside: Terminology

- Non-volatile RAM (NVRAM)
- Non-volatile memory (NVM)*
- Persistent memory

** Except flash memory*

➔ The same thing: durable + byte-addressable

Persistent Memory Properties

- Byte-addressable, durability
  - + Energy efficient
  - + Scales, high density, cheaper

Can be used to build both memory and storage

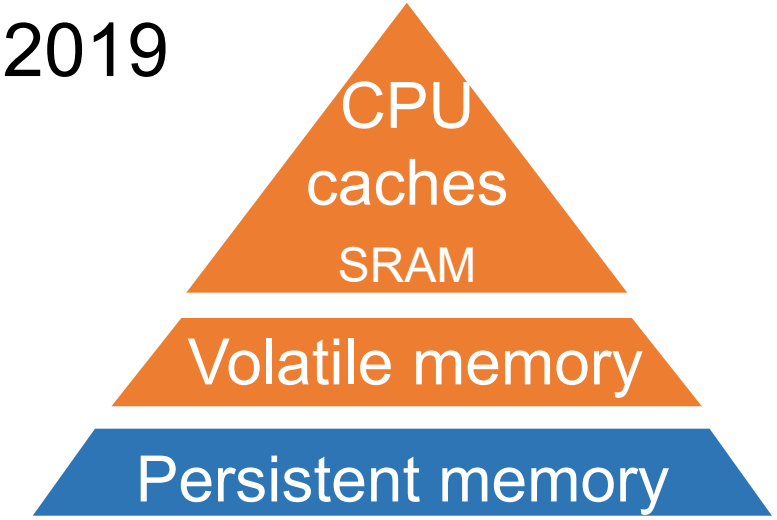
Can be faster or slower than DRAM

- Performance varies depending on particular memory technology
  - E.g., STT-RAM as an alternative to SRAM cache
    - Tradeoffs between persistence/retention/speed/energy profile [9]

- In most cases, biased towards PCM/3D XPoint (Optane) and compare with DRAM:
  - + Energy efficient
  - + Scales, high density, cheaper
  - – Higher read/write latency than DRAM
  - – Read/write asymmetry
  - – Limited lifetime (but not a big concern)

Persistent Memory

- Available today: Intel 3D XPoint (Optane) since 2019
  - But winding down, more on this later
  - (future slides – Optane-specific marked with )
- Other candidates
  - Work-in-progress, or
  - Failed previous attempts, or
  - Do not scale (yet), or
  - Do not scale economically, or



Persistent Memory

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Aside: Non-Volatile DIMMs (NVDIMMs) [9]

- DRAM + flash + supercapacitor
  - Flush data to flash upon power failure, load back when powered on again
  - SNIA standardized: NVDIMM-F, NVDIMM-N, etc.
- **Also "persistent" and available today but:**
  - **Doesn't scale (due to DRAM)**
  - Same speed as DRAM (NVDIMM-N)
  - Expensive

➔ A major research vehicle pre-Optane

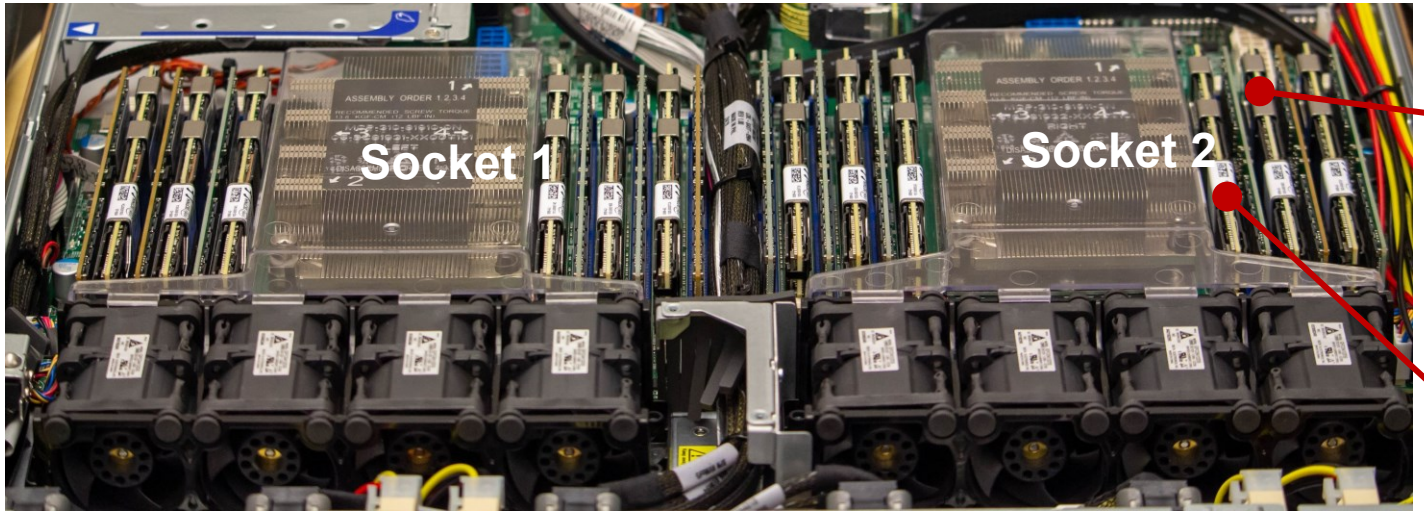
Optane PMem

Aka “Optane DCPMM”

- High capacity – easily TB level
- “Economical” (more later)
  - ~CA$750 / 128GB Optane PMem
  - ~CA$2000 / 128GB DRAM

~July 2019

1	Intel Xeon Gold 6252 24-Core Server	CA$26243.32
	2x Intel Xeon Gold 6252 24-Core 48-Thread 2.10 GHz 35.75M Cache Server Processor	
	384GB (12x 32GB) DDR4-2666 ECC Registered RDIMM	
	1x Intel D3-S4610 240GB SATA SSD - 3D TLC 2.5" 3 DWPD	
	12x Intel 128GB DDR4-2666 Optane Memory - AEP 3DXP DCPMM Optane Memory	

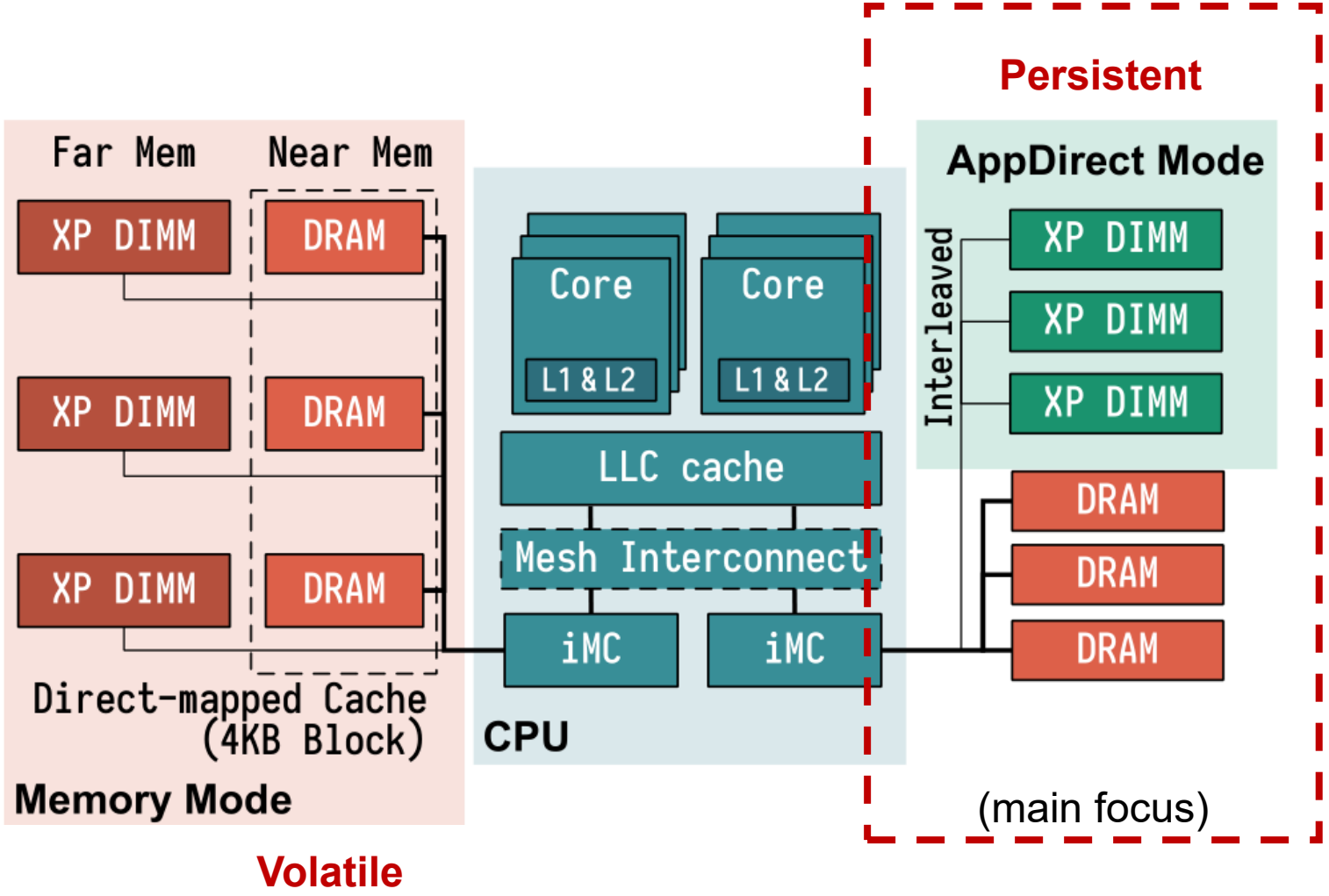


DRAM DIMMs
75ns latency
BW >60-100 GB/s
(16 threads)

Optane PMem 100
300ns read latency
Read BW 7.4-40GB/s
Write BW 5.3-10GB/s
(16 threads)

PMem 200: ~30% higher

System Architecture and Operation Modes



[CEATEC] Rohm Demonstrates Nonvolatile CPU, Power Consumption Cut by 90%

Motoyuki Ooishi, Nikkei Electronics — Oct 4, 2007

Like Share 0 Tweet 0 Print

Rohm Co. Ltd. prototyped a nonvolatile CPU and exhibited it at CEATEC Japan 2007. The company prototyped a 4-bit microcomputer and made it nonvolatile by adding ferroelectric memory chips to all of the about 300 registers.

This time, the company demonstrated a breakout game by using a nonvolatile CPU, comparing with the case in which an existing CPU is used.

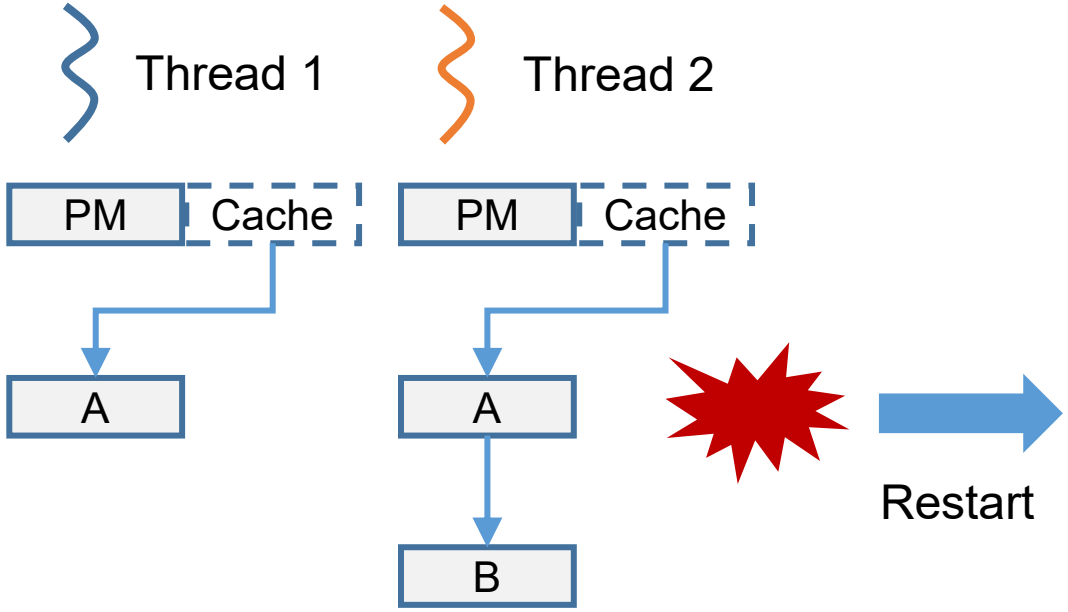
The demonstration of a breakout game

Still volatile CPU caches

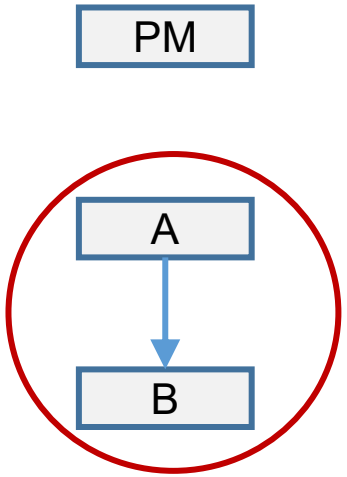
[41] J. Yang et al. An Empirical Guide to the Behavior and Use of Scalable Persistent Memory

Programming Model without eADR

- ADR: Asynchronous DRAM Refresh
  - Includes write buffer and PMem, but not the CPU caches



Case 1: Optane PMem 100, pre- Ice Lake
Actually persisted state:



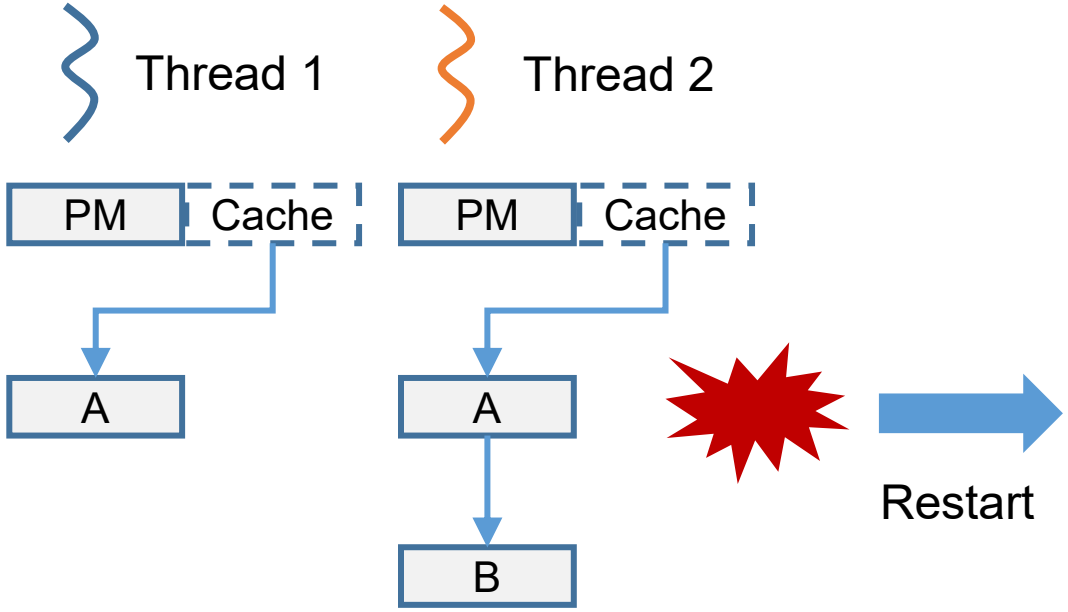
Unreachable

Need explicit cacheline writeback (clflush, clflushopt, clwb)

Visible != durable

Programming Model with eADR

- eADR: Enhanced Asynchronous DRAM Refresh
  - Includes write buffer and PMem, *and* the CPU caches



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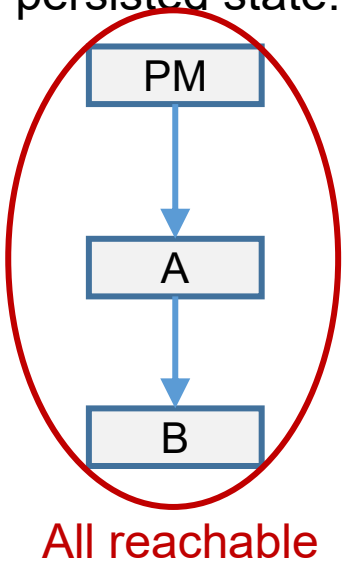


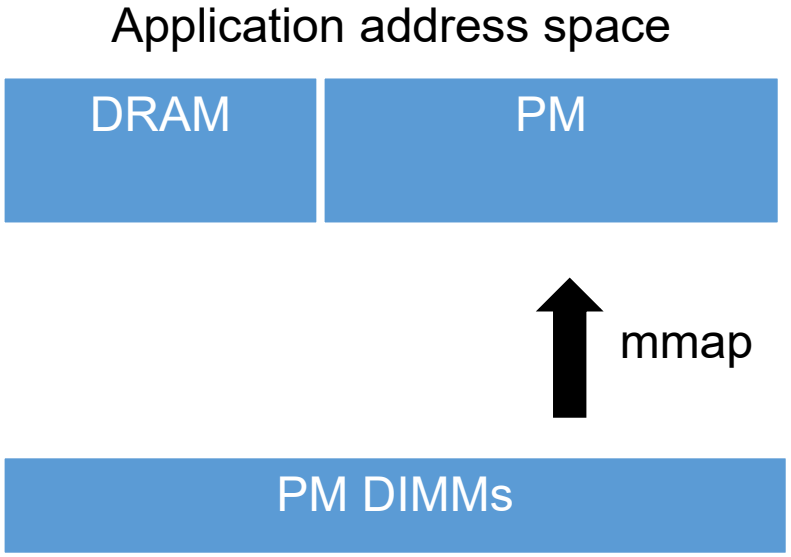
All reachable

Enhanced ADR – no need to flush; fence still needed

Visible == durable

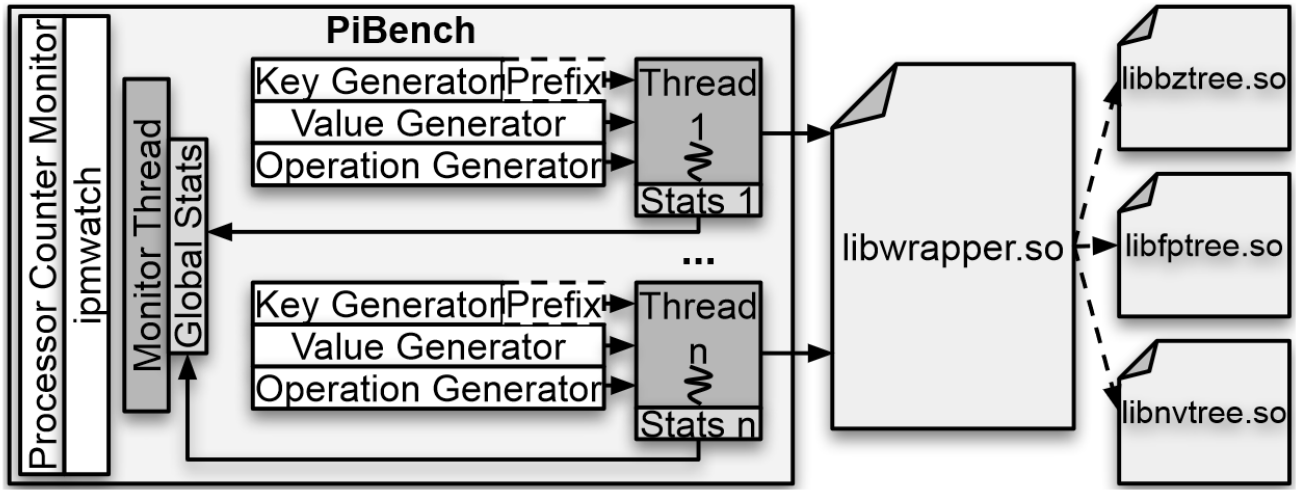
Software Tools: PM Programming

- Access via load/store instructions
- Add fences and flushes (without eADR)
- Guaranteed: 8-byte atomic write
  - Atomics (CAS, XCHG, etc.) also work
- Allocating/deallocating PMem
  - `malloc` doesn't work!
  - Handling (persistent) memory leaks
  - Solutions
    - Ownership transfer protocol: application provides a tracked location for allocator
    - "Transactions" (for durability): use logging
- Guaranteed by PM programming libraries
  - Intel PMDK (https://pmem.io/pmdk)
  - Research: NVHeaps [10], Mnemosyne [11], PMwCAS [12]



Software Tools: Index Evaluation

- PiBench [18]
  - Unified benchmarking framework
  - Pluggable index shared lib
  - Issue synthetic workloads
    - R/W ration, varying core count
  - Stats information
    - Throughput, tail latency, bandwidth



  - Not limited to PM; used by various recent index work
  - Open-source:
    - https://github.com/sfu-dis/pibench

Part 2: PM Range Indexes

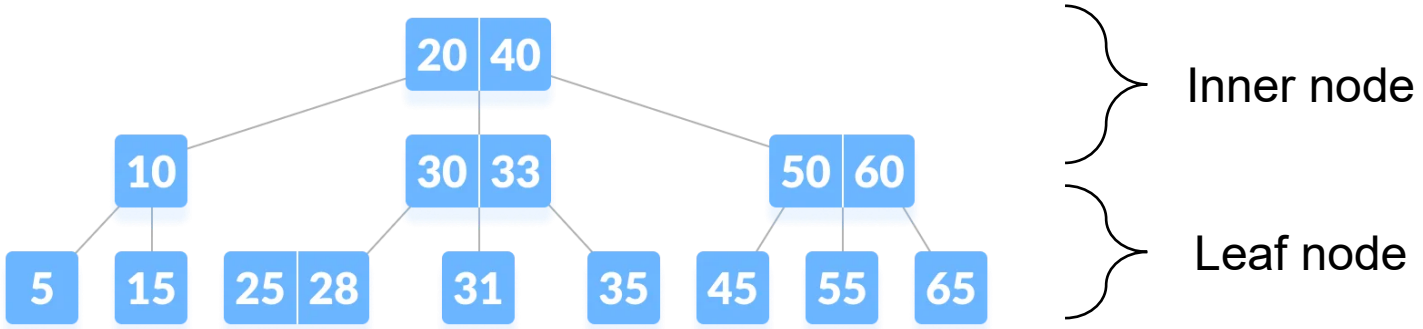
Part Two: Outline

- Common range index choices: B+-Tree vs Trie
- Range indexes on PM
  - Pre-Optane PM indexes
  - State-of-the-art PM indexes

Btree vs Trie

BTree:

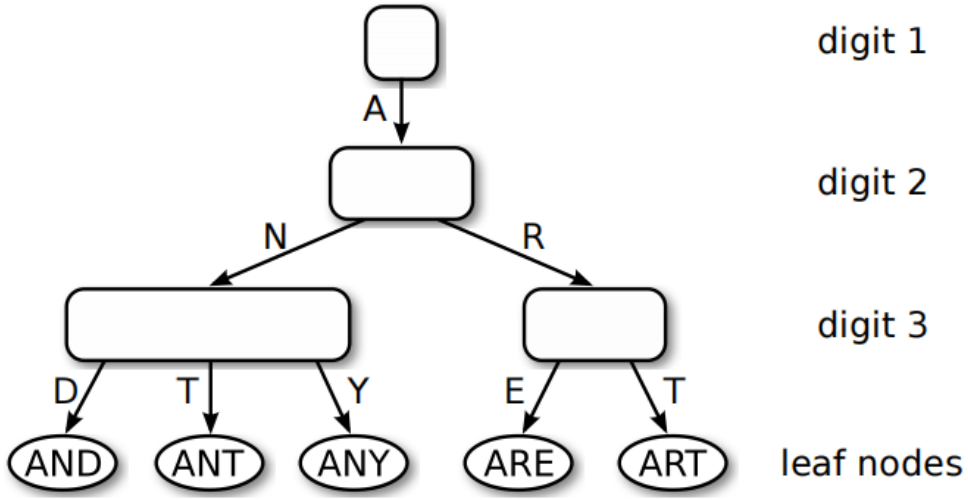
- O(log n) access time
- Range scan locality
- Variable-length key support



https://cdn.programiz.com/sites/tutorial2program/files/b-tree.png

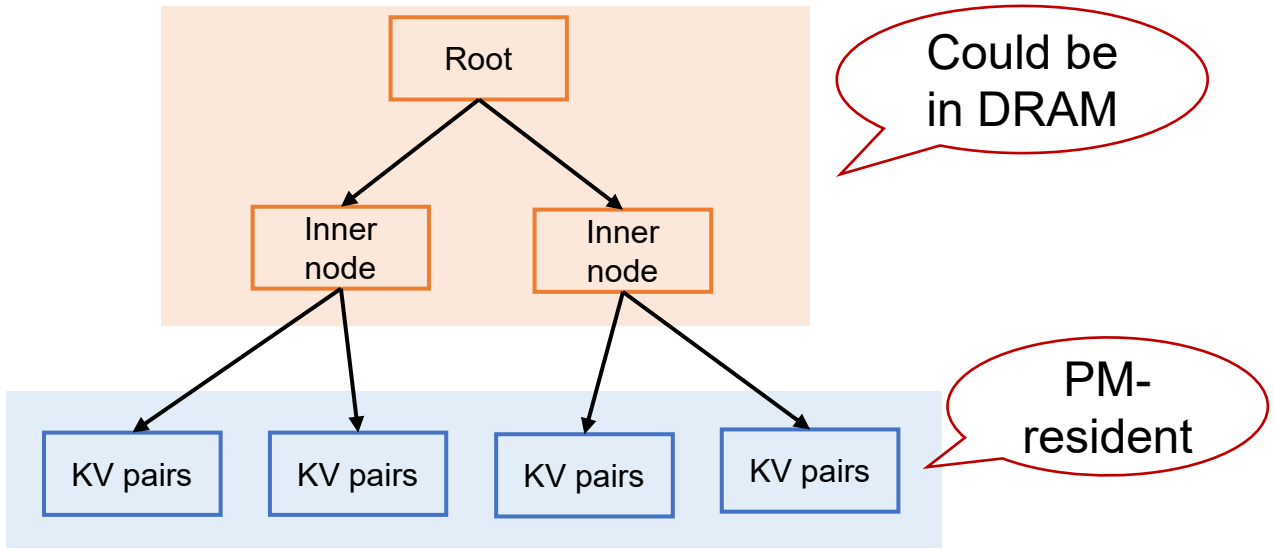
Trie:

- O(L) access time (L = key length)
- Variable-length key support
- Pointer chasing during scan



[13] The Adaptive Radix Tree: ARTful Indexing for Main-Memory Databases

Range Indexes on Persistent Memory



- No serialization/deserialization
- Directly persist on PM
- Tailor-made for Optane DCPMM
- (Near) Instant recovery

Challenges:

- Consistency - 8-byte atomic write
- Performance - scarce write bandwidth
- Recovery - avoid persistent memory leak

Key optimization goal:

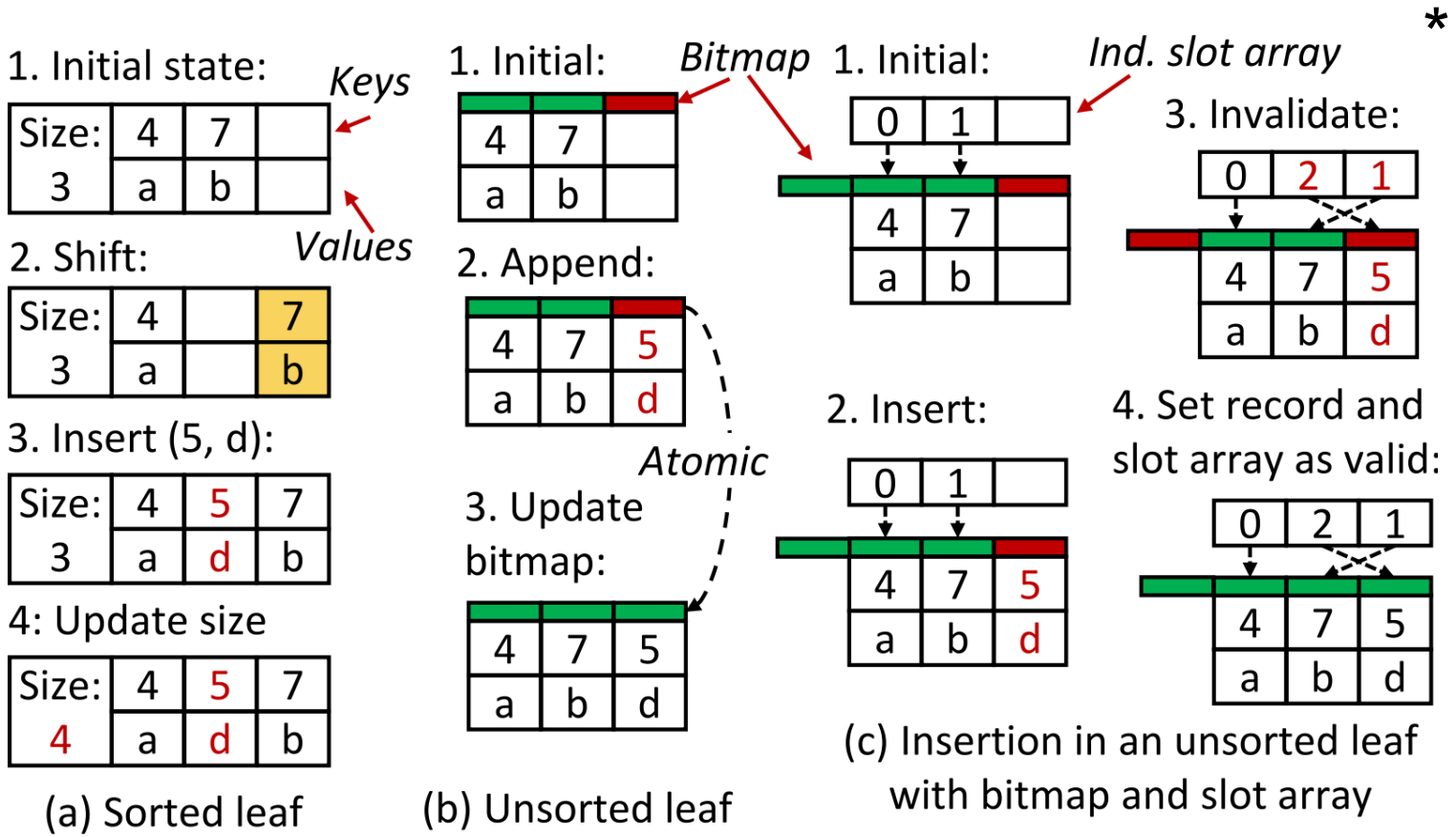
- Reduce PM accesses ➔ higher performance

Perhaps 10s-100s of proposals by now

- Even before real devices appeared
- Even more with real devices

Pre-Optane: wBTree [14]

- Unsorted leaf with atomic update
- Indirection array
  - 1 bit to indicate validity
- Logging during split
- Single-threaded

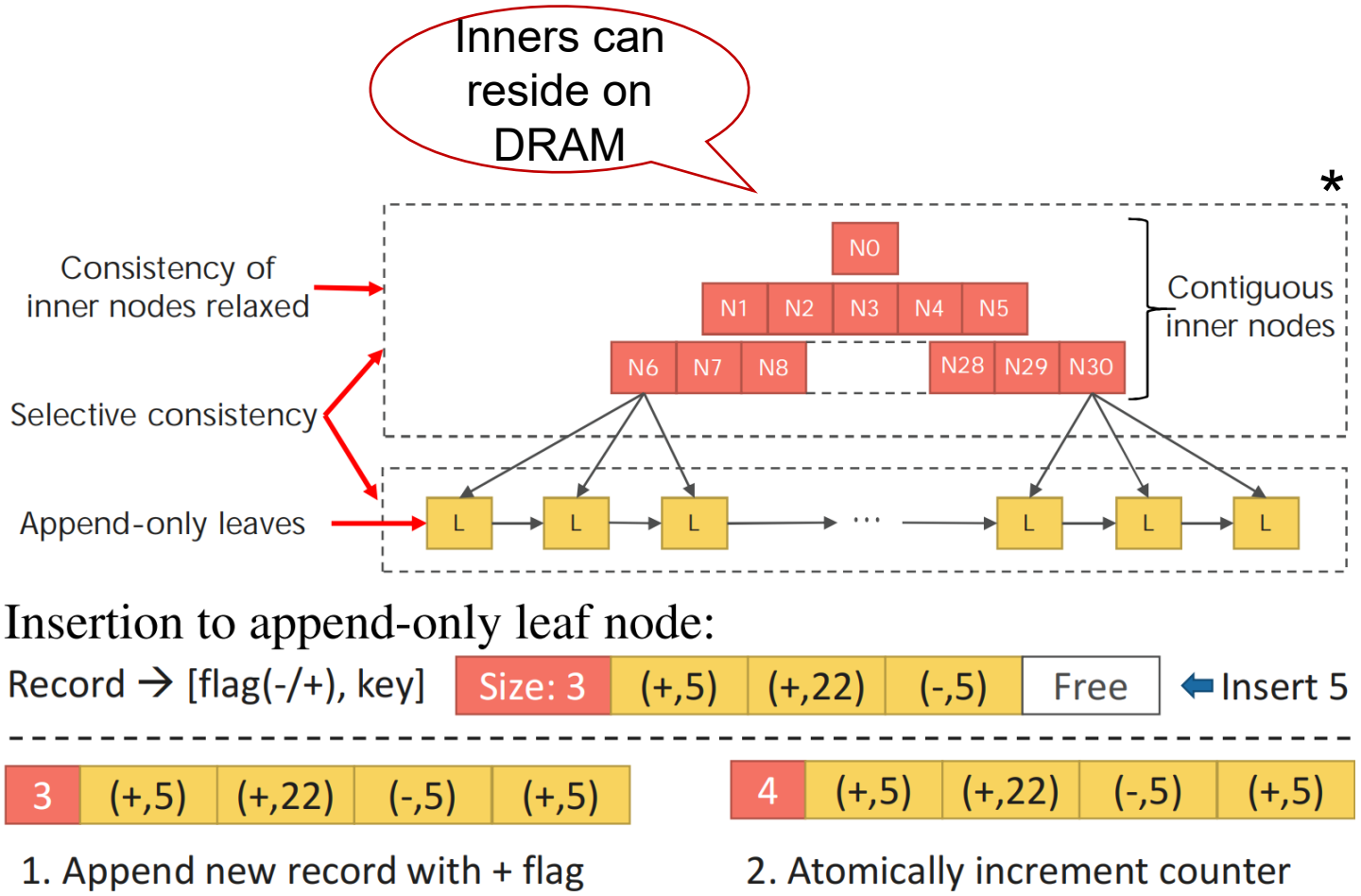


*

[14] Persistent B⁺-trees in non-volatile main memory, *VLDB 2015*

Pre-Optane: NVTree [15]

- Selective consistency
- Contiguous inner nodes
  - Gaped array to absorb split
- Unsorted leaf
  - Append-only strategy
- Scan backwards to find key

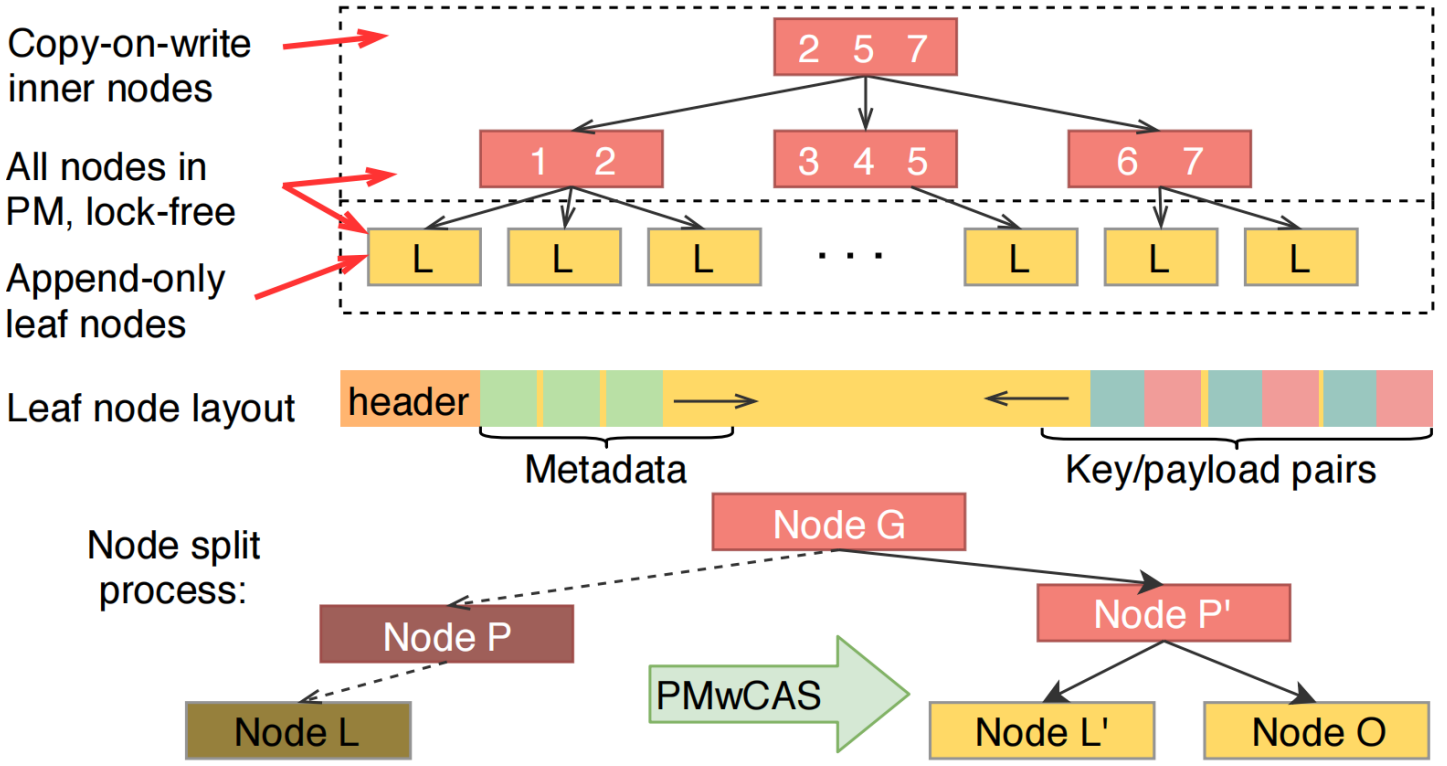


[15] NV-Tree: Reducing Consistency Cost for NVM-based Single Level Systems, *FAST 2015*

Pre-Optane: BzTree [16]

- Lock-Free (PMwCAS – Persistent Multi-word Compare And Swap)
- Unsorted leaf
  - Periodically sort records
- Search method
  - Binary search sorted area
  - Linear search unsorted area

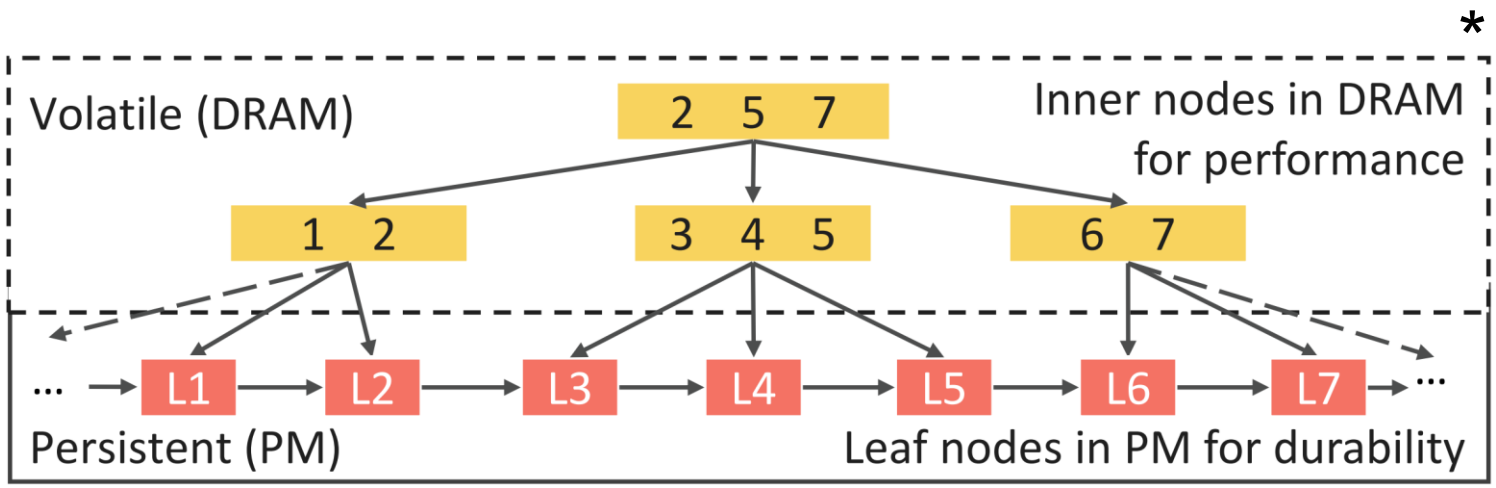
*



[16] Bztree: a high-performance latch-free range index for non-volatile memory, *VLDB 2018*

Pre-Optane: FPTree [17]

- Selective persistence
- Unsorted leaf + fingerprints (one byte hash of key)
- Selective concurrency
  - HTM for inner node update
  - Locks for leaf node update



[17] FPTree: A Hybrid SCM-DRAM Persistent and Concurrent B-Tree for Storage Class Memory, *SIGMOD 2016*

Pre-Optane PM Range Indexes (Pre-2019) [18]

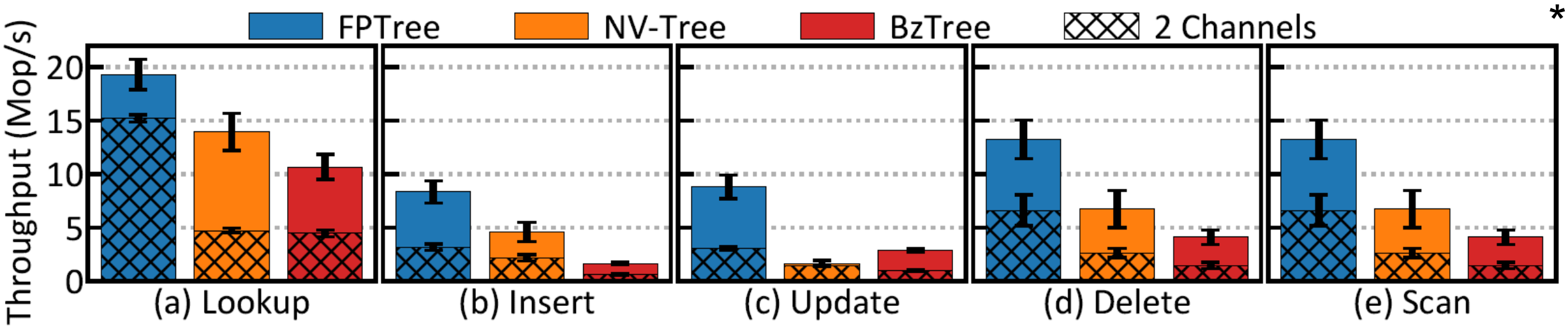
- Proposed under emulation, evaluated under Optane PMem

Index	Architecture	Node Architecture	Concurrency
wBTree [VLDB '15]	PM-only	Unsorted; Indirection array	Single-threaded
NV-Tree [FAST '15]	DRAM + PM	Unsorted leaf; Inconsistent inner node	Locking
FPTree [SIGMOD '16]	DRAM + PM	Unsorted Leaf; Fingerprints	HTM (inner) + Locking (leaf)
BzTree [VLDB '18]	PM-only	Partially unsorted leaf	Lock-free + PMwCAS

[18] Evaluating Persistent Memory Range Indexes, *VLDB 2020*

Pre-Optane PM Range Indexes (Pre-2019) [18]

- 6 channels (solid + shadow) vs. 2 channels (shadow only)
- 23 threads



Key takeaways: save write bandwidth + leverage DRAM + fingerprinting

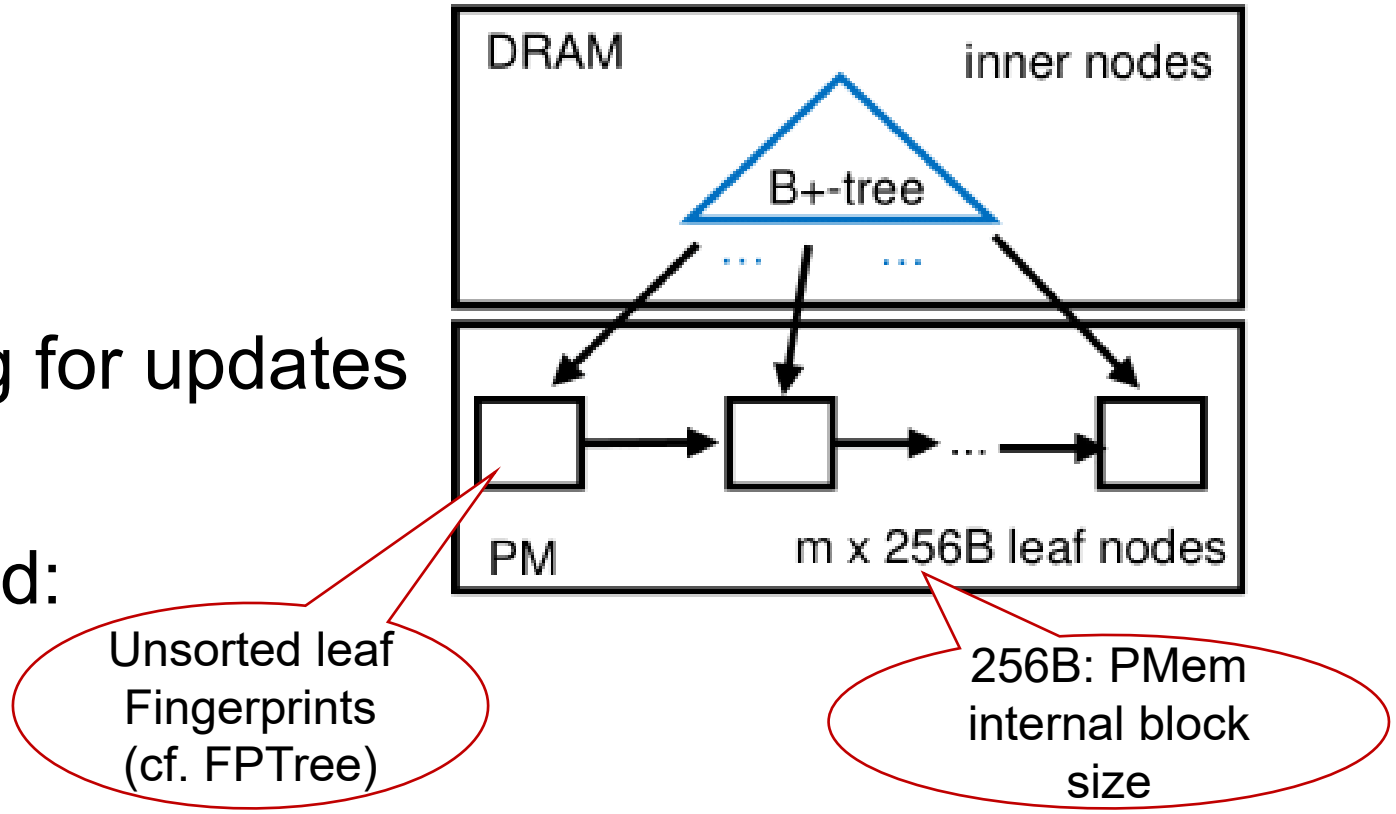
[18] Evaluating Persistent Memory Range Indexes, *VLDB 2020*

Into the Era of Optane 2019-2022

- Even more indexes
  - 10s of papers in VLDB/SIGMOD/SOSP, etc.
- More index structure choices
  - B+-tree, trie, hybrid, learned
- Functionality
  - NUMA-awareness, variable-length key support, etc.

Optane: LB+-Tree [19]

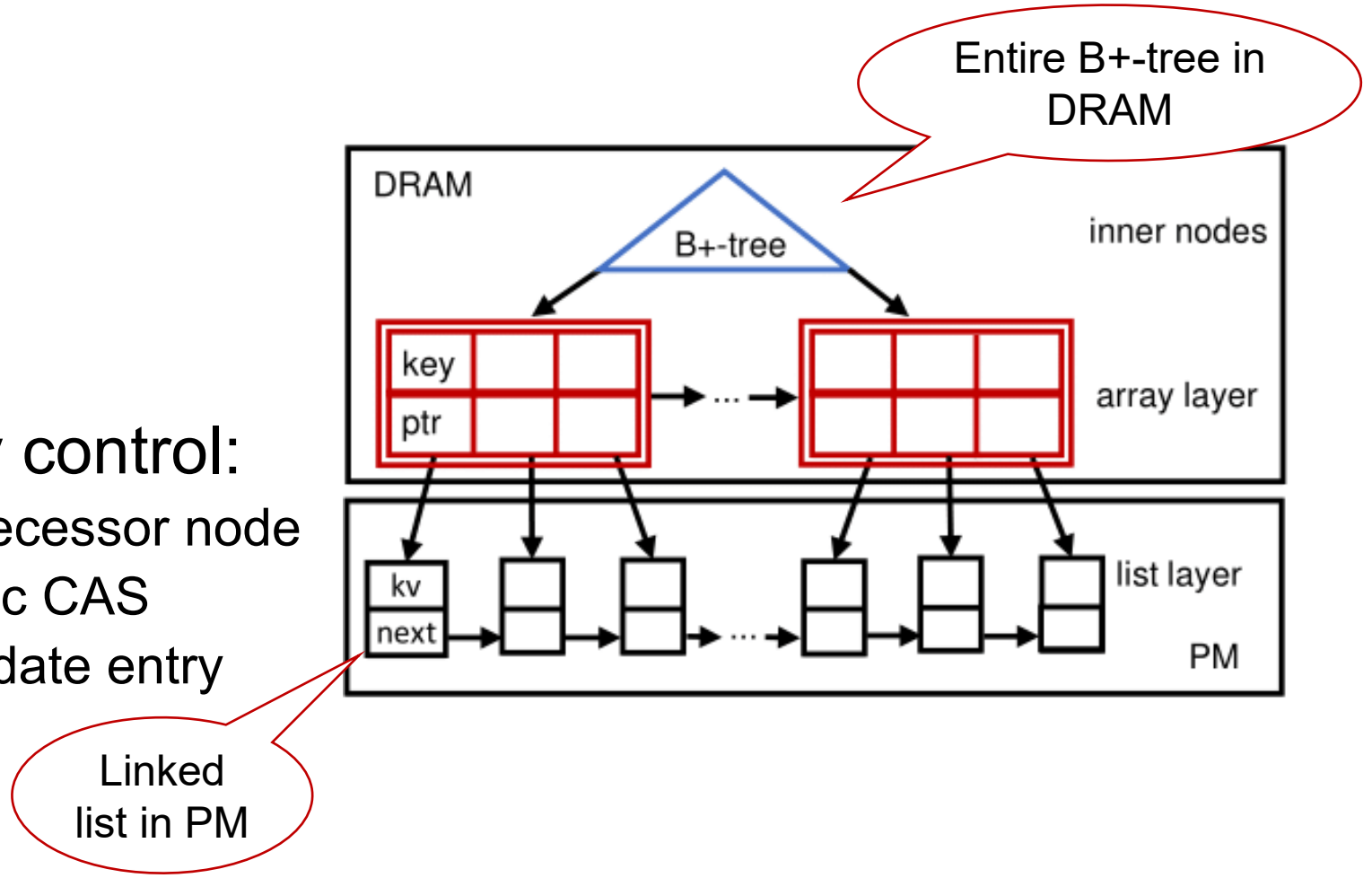
- B+-tree based
  - Inner nodes in DRAM
  - Leaf nodes in PM
- HTM for traversal, locking for updates
- + New techniques to avoid:
  - Excessive PM writes
  - Logging overhead



[19] LB+-Trees: optimizing persistent index performance on 3DXPoint memory, *VLDB 2020*

Optane: µTree [20]

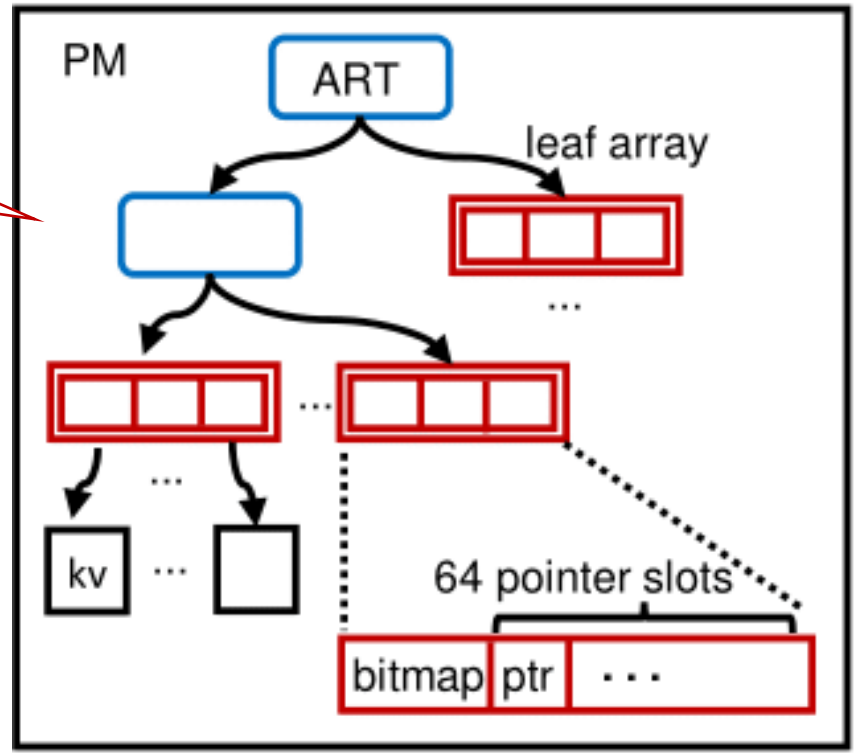
- B+-tree based
- Optimized for tail latency
- Coordinated concurrency control:
  - Traverse B+-Tree, find predecessor node
  - Update list layer using atomic CAS
  - Lock array layer leaf and update entry



[20] µTree: a Persistent B+-Tree with Low Tail Latency, *VLDB 2020*

Optane: ROART [21]

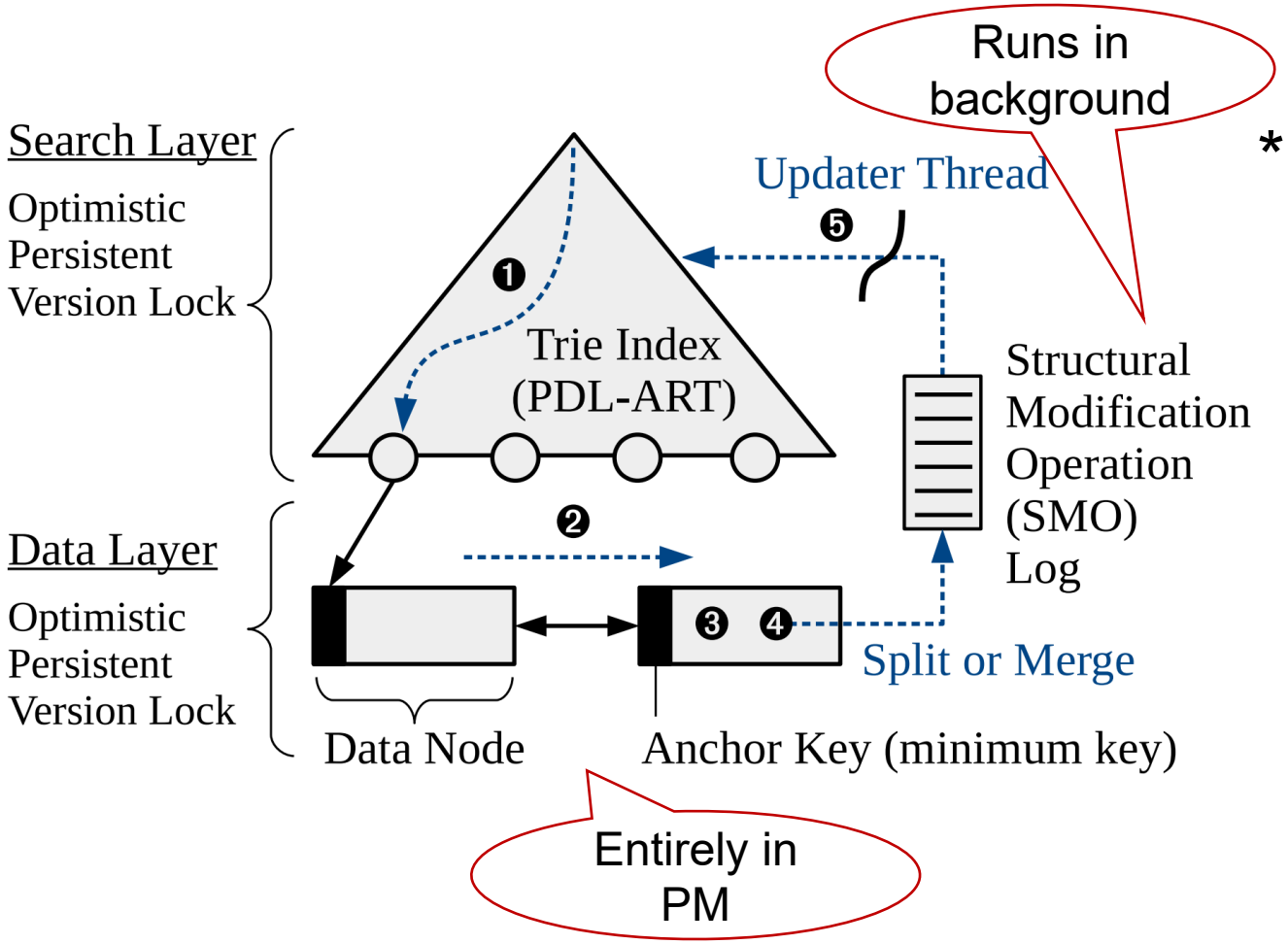
- Based on ART
- Optimized for range scan
- Compact subtrees into leaf arrays
- Delayed Check Memory Management
- Concurrency
  - ART-ROWEX
  - Non-temporal stores



[21] ROART: Range-query Optimized Persistent ART, *FAST 2021*

Optane: PACTree [22]

- Trie-based (ART)
- Search layer: persistent trie
- Data layer: linked list of leaves
- Asynchronous update
  - SMOs by background threads
- NUMA-optimized
  - Per-node PM pool

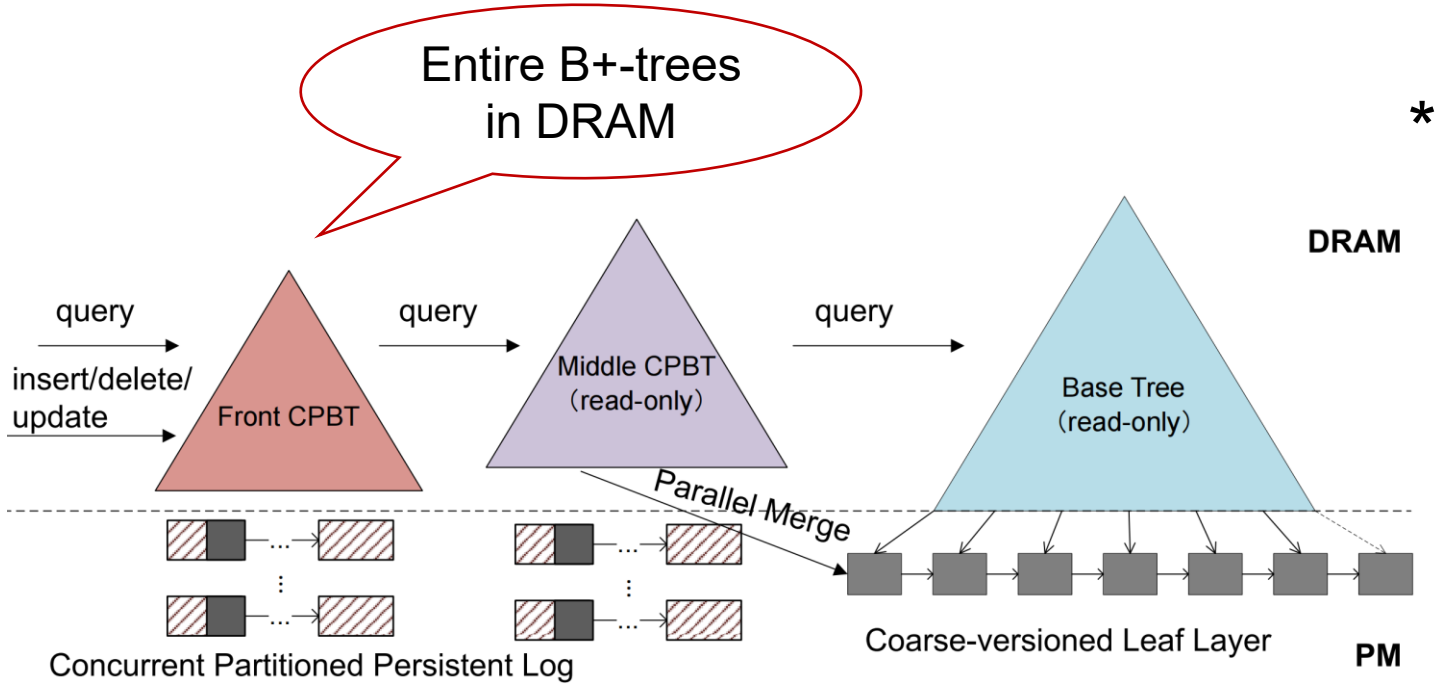


[22] PACTree: A High Performance Persistent Range Index Using PAC Guidelines, *SOSP 2021*

Optane: DPTree [23]

- Hybrid B+-tree and trie

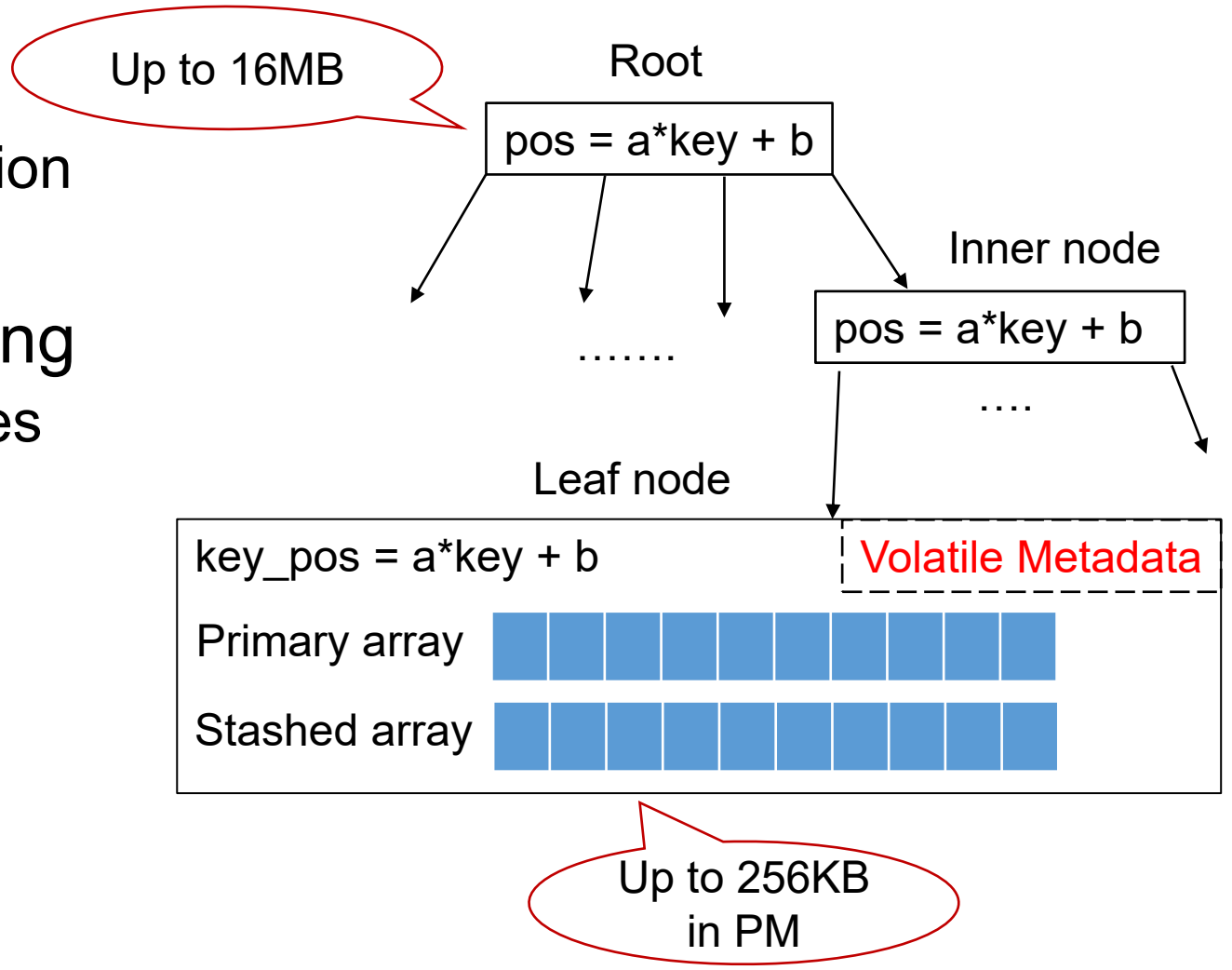
- Front Buffer Tree
  - B+-tree
  - All modifications with logging
- Base Tree
  - Read-only trie for inner nodes
  - B+-Tree style leaf nodes
  - Accumulates front buffer trees
- Lookup will traverse all trees



[23] DPTree: differential indexing for persistent memory, *VLDB 2020*

Optane: APEX [24]

- Learned, based on ALEX [25]
  - Linear function to predict key location
- Probe-and-Stash collision handling
  - Probe primary array up to 16 entries
  - If empty slot found, insert into PA
  - Otherwise insert to stashed array
- Concurrency
  - Inner: Lock-free traversal
  - Leaf: Optimistic locking



[24] APEX: A High-Performance Learned Index on Persistent Memory, VLDB 2022
[25] ALEX: An Updatable Adaptive Learned Index, SIGMOD 2020

Optane-Era PM Range Indexes (2019-2022) [26]

	Architecture	Node structure	Concurrency
LB+-Tree [VLDB 20]	B+-tree; DRAM (inner) + PM (leaf)	Unsorted leaf; fingerprints; extra metadata	HTM (traversal) + locking (update)
uTree [VLDB 20]	B+-tree; DRAM (B+-tree) + PM (leaf)	Sorted	Locking (array layer) + lock-free (list layer)
DPTree [VLDB 20]	Hybrid; DRAM (B+-tree, trie inner) + PM (trie leaf)	Unsorted leaf; fingerprints; indirection; extra metadata	Optimistic lock + async update
ROART [FAST 21]	Trie; PM-only	B+-tree like unsorted leaf; fingerprints	ROWEX
PACTree [SOSP 21]	Trie; PM-only (conceptually DRAM+PM)	Unsorted leaf; fingerprints; indirection	Optimistic lock + async. Update
APEX [VLDB 22]	Learned index; PM-mostly (metadata in DRAM)	Partially unsorted leaf; fingerprints; stashed array	Lock-free traversal + optimistic locking
FPTree [SIGMOD 16]	DRAM (inner nodes) + PM (leaf nodes)	Unsorted leaf nodes; fingerprints	HTM (inner nodes) + locking (leaf nodes)

B+-Trees: extensive use of DRAM

Tries: B+-Tree styled leaf

(mostly) unsorted + Search techniques

(mostly) optimistic

Support var-keys naturally

NUMA-optimized

Learned

Detailed performance comparison: Evaluating Persistent Memory Range Indexes: Part Two, VLDB 2022

Part 3: PM Hash Tables

Part Three: Outline

- Range indexes vs hash tables
- Representative hashing schemes
- New challenges and new proposals
- Design summary

Range Indexes vs. Hash Tables

	Range Indexes	Hash Tables
Pros	• Good at range queries • Smooth growth (collision-free)	• Good at point queries • Average O(1) time complexity for insertion/deletion/search
Cons	• Average O(logN) time complexity for insertion/deletion/search	• Lack support for range queries • Unavoidable collisions

PM Range Indexes vs. PM Hash Tables

	Range Indexes	Hash Tables
Pros	Common frenemy: PM access!	
Cons		

PM Range Indexes vs. PM Hash Tables

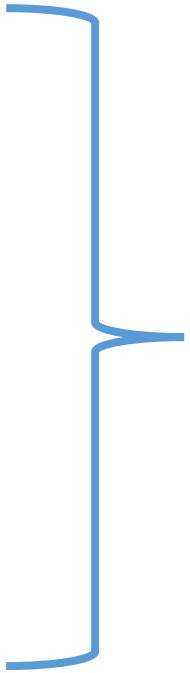
	Range Indexes	Hash Tables
Pros		
Cons	**Common challenges:** #1 Consistency – 8-byte atomic write #2 Performance – scarce write bandwidth #3 Recovery – avoid persistent memory leak	

Recap

A hash table implementation = hashing scheme + hash function

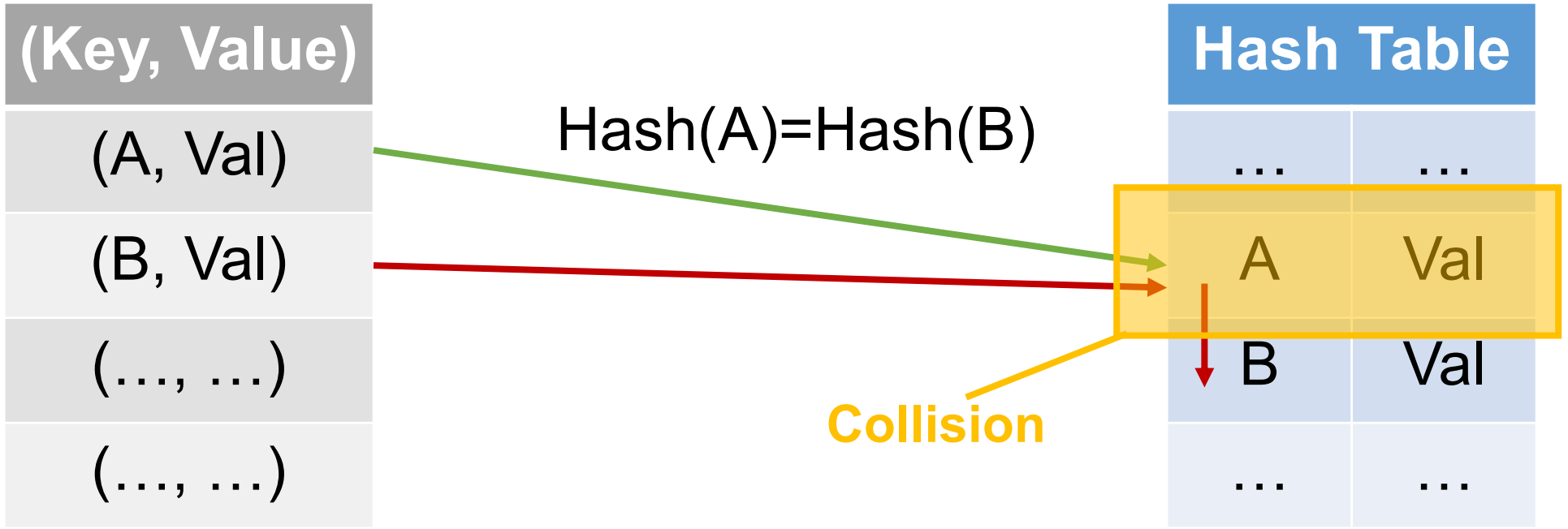
Static hashing schemes
- Linear probing
- Cuckoo hashing
- …

Dynamic hashing schemes
- Extendible hashing
- Linear hashing
- …

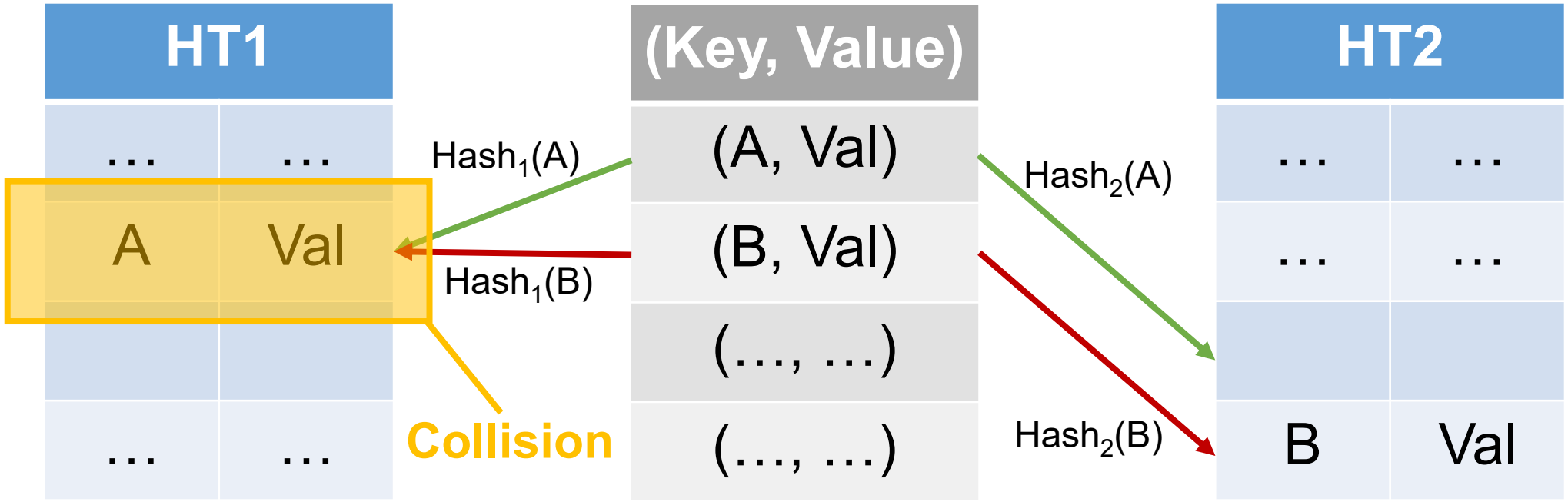


Most PM hash tables are also based on

Static Scheme – Linear Probing



Static Scheme – Cuckoo Hashing



From Static to Dynamic

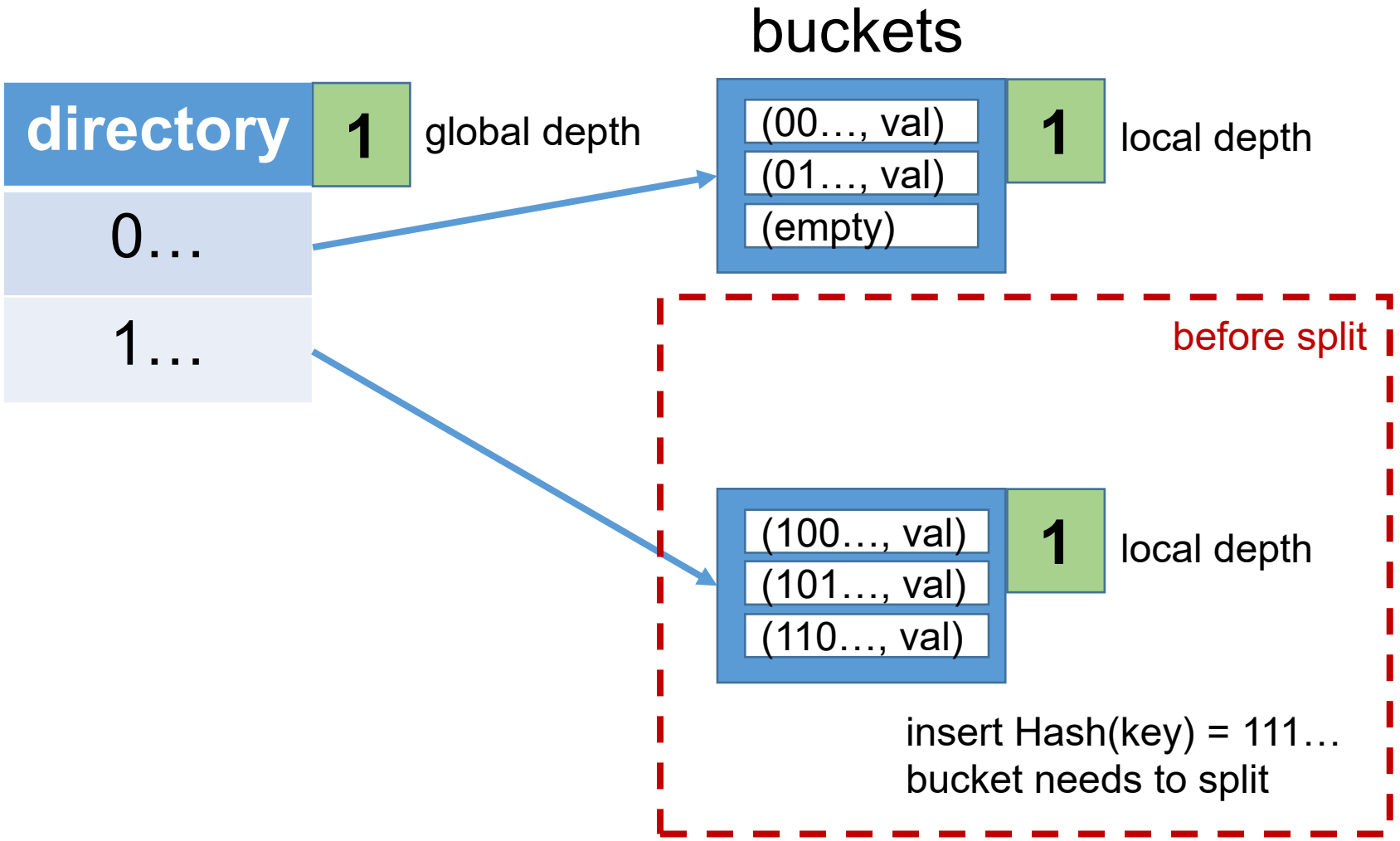
So, we need to rebuild the entire hash table when it is full.

But, rebuilding a hash table is very expensive even for DRAM.

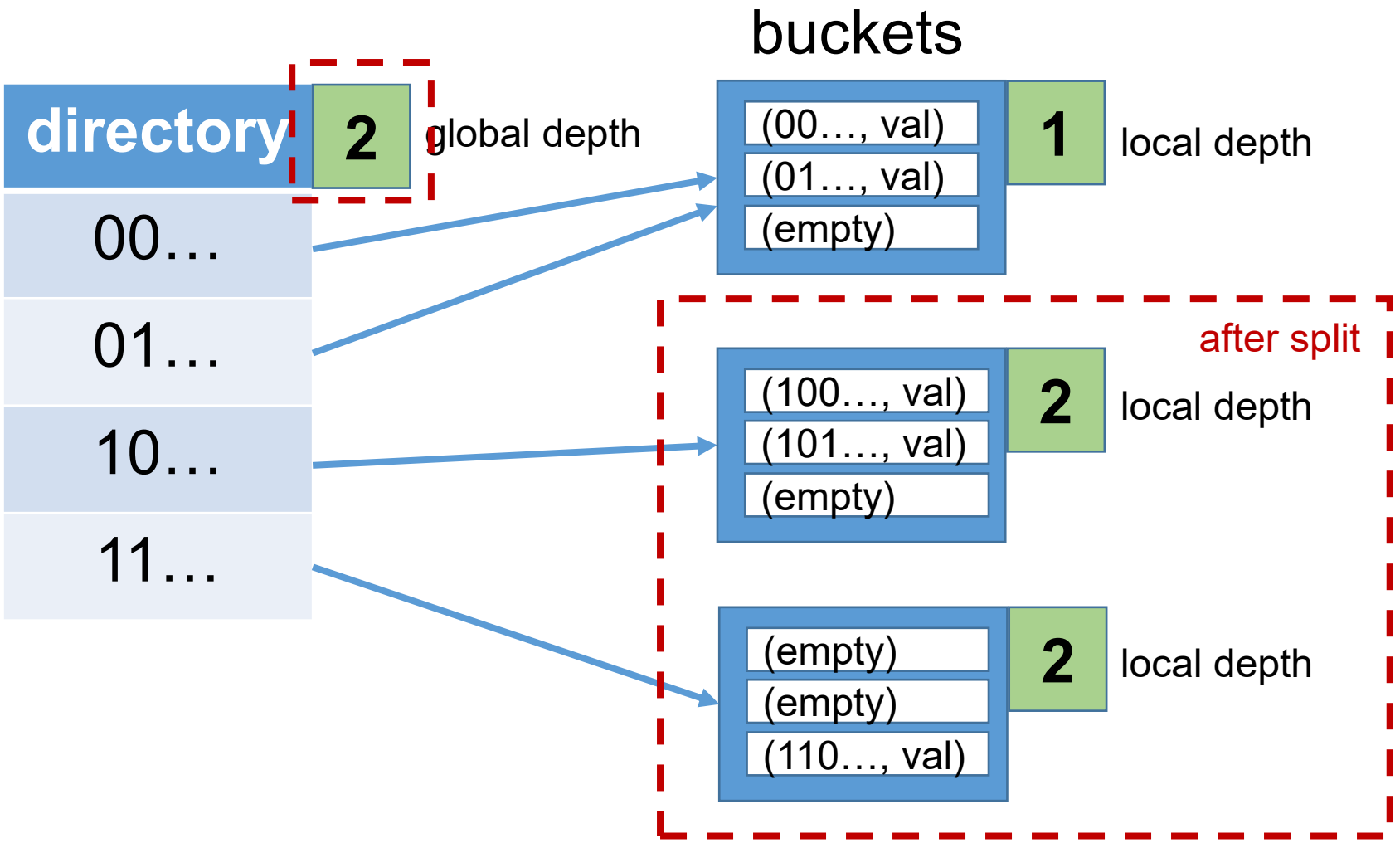
How to smooth out the process?

Dynamic hashing schemes.

Dynamic Scheme – Extendible Hashing



Dynamic Scheme – Extendible Hashing



Dynamic Scheme – From Extendible to Linear

So, we need to double the size of the directory when a bucket splits.

Oof, can we make the growth even smoother?

Linear hashing scheme. (Similar challenges in practice)

Hash Tables on PM

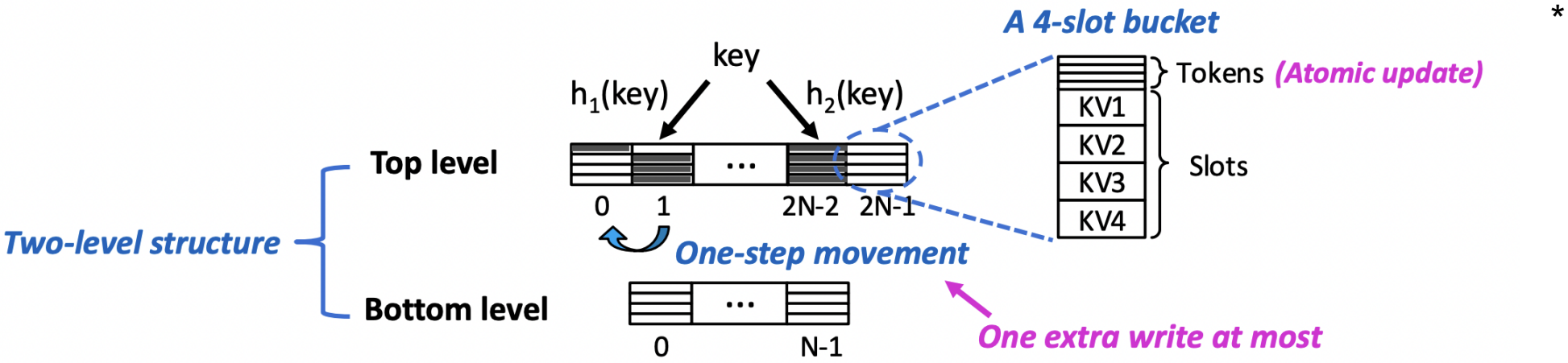
- Static hashing variants
  - Level hashing [27]
  - Clevel [28]

- Dynamic hashing variants
  - Cacheline-conscious extendible hashing (CCEH) [29]
  - Dash [30]

[27] Write-Optimized and High-Performance Hashing Index Scheme for Persistent Memory, OSDI ’18
[28] Lock-free Concurrent Level Hashing for Persistent Memory, ATC ’20
[29] Write-Optimized Dynamic Hashing for Persistent Memory, FAST ’19
[30] Dash: scalable hashing on persistent memory, VLDB ’20

Pre-Optane, Static: Level Hashing [27]

- Emulation-based bucketized cuckoo hashing
- Challenge #1: heavyweight consistency guarantee
  - Overcome by atomic token update
- Challenge #2: excessive PM write
  - Overcome by two-level bucketized hash table & in-place resizing



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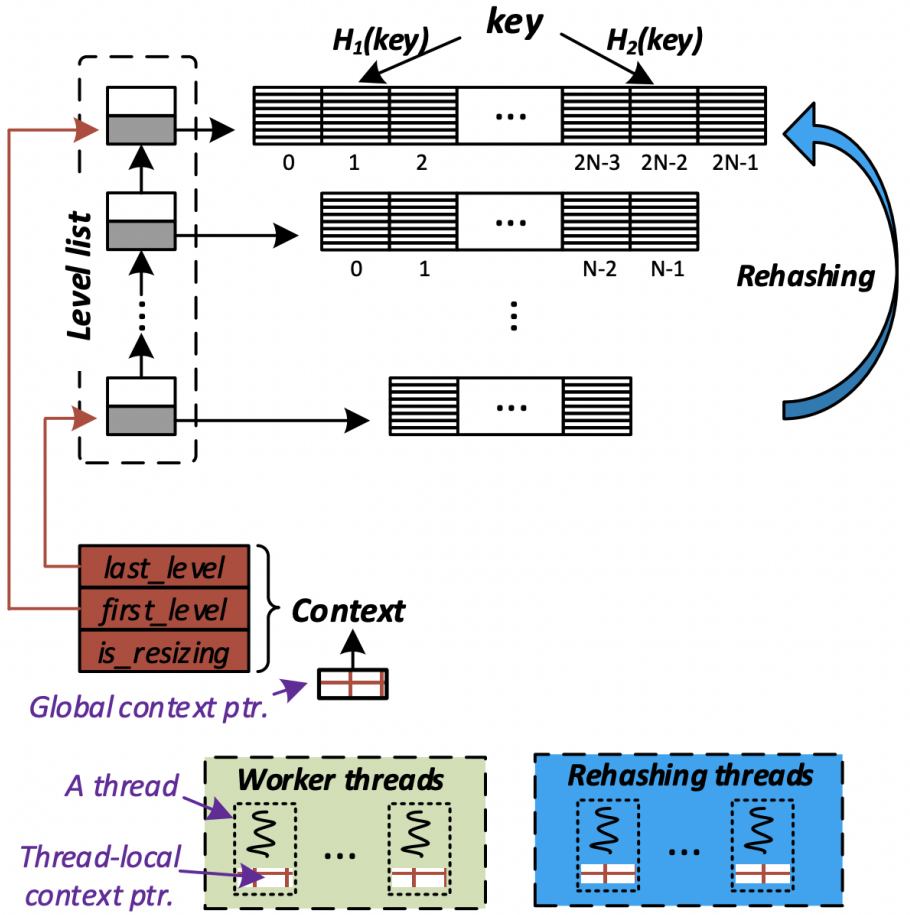
[27] Write-Optimized and High-Performance Hashing Index Scheme for Persistent Memory, OSDI '18

**https://www.usenix.org/system/files/atc20-paper227-slides-chen.pdf*

Optane, Static + Resizing: Clevel [28]

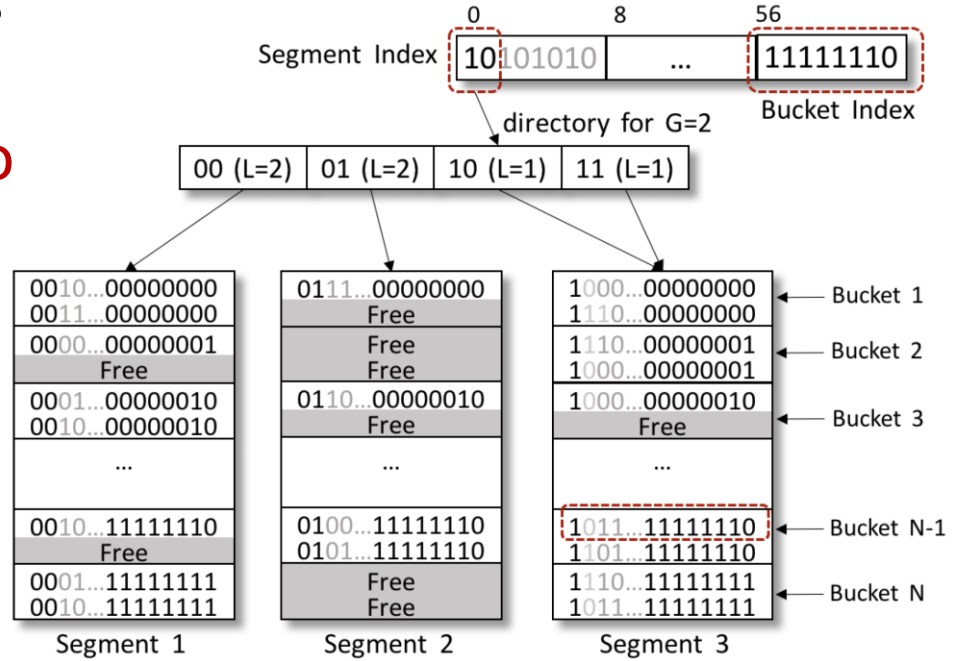
- Lock-free concurrent level hashing implemented on Optane PMem
- **Based** on level hashing with new challenges!
- Challenge #1: performance degradation during resizing
  - Overcome by replacing coarse-grained locks in level hashing with async rehashing
- Challenge #2: poor scalability of level hashing
  - Overcome by lock-free search/insertion/update/deletion



[28] Lock-free Concurrent Level Hashing for Persistent Memory, ATC '20

Pre-Optane, Extendible: CCEH [29]

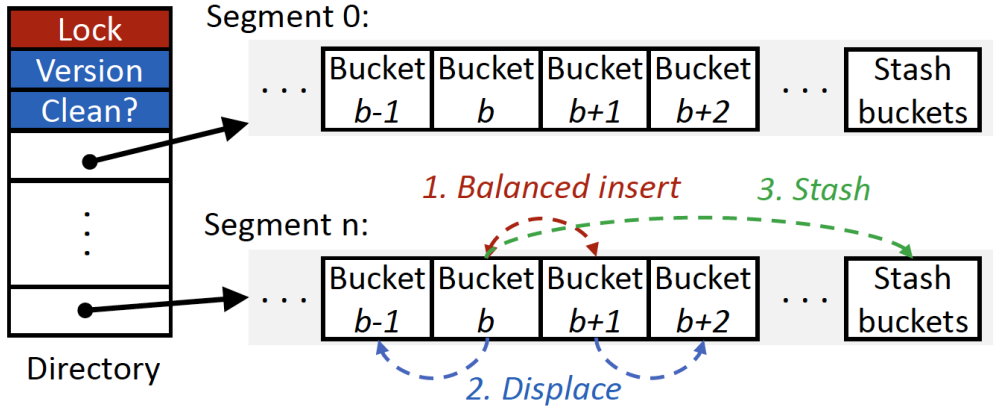
- Emulation-based extendible hashing
- Challenge #1: reducing cacheline accesses
  - Overcome by the three-level structure which makes sure that record can be found within two cacheline accesses
- Challenge #2: crash consistency
  - Overcome by keeping track of split history in the split buddy tree and reducing dirty writes through lazy deletion



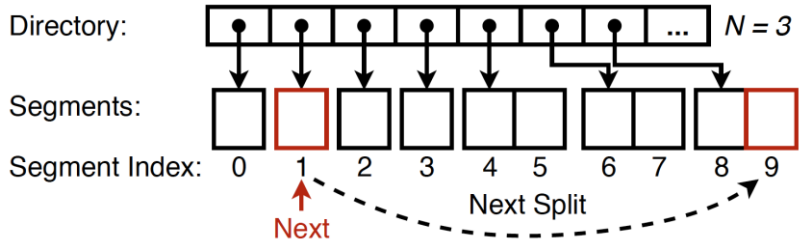
[29] Write-Optimized Dynamic Hashing for Persistent Memory, FAST '19

Optane, Extendible/Linear: Dash [30]

- Optane-based extendible/linear hashing
- Challenge #1: excessive PM read
  - For Optane, read latency > write latency
  - Overcome by fingerprint
- Challenge #2: heavyweight concurrency control (read-write lock)
  - Overcome by optimistic lock
- Challenge #3: load factor optimization
  - Overcome by bucket load balancing
- Challenge #4: instant recovery
  - Overcome by lazy recovery



(a) Overview of Dash-EH



(b) Overview of Dash-LH

[30] Dash: Scalable Hashing on Persistent Memory, VLDB 2020

PM Hash Tables: Design Summary

	Level Hashing	Clevel	CCEH	Dash
Reduce PM write	☑	☑	☑	☑
Reduce PM read				☑
Lightweight concurrency control		☑		☑
Lightweight consistency guarantee	☑	☑	☑	☑
Load factor optimization	☑	☑		☑
Resizing optimization	☑	☑		
NUMA optimization				
Instant recovery	☑	☑		☑
Variable-length key support				☑

Part 4: Implications and Outlook

Other Related/More-Recent Work

- This tutorial by no means exhaustive
  - Still fast evolving

- Some more recent PM indexes
  - Tree leveraging eADR: NB-Tree [34]
  - Hash table: Plush [35]

- PM key-value stores
  - Viper [38], FlatStore [39], Halo [40], etc.

- PMem-based full systems
  - Tair [36], OpenMLDB [37]

NEWS

Intel pulls the plug on Optane

Intel will wind down its storage class
elsewhere, while still supporting curr

By **Adam Armstrong,** News Writer

Home > Storage

Intel To Wind Down Optane Memory Business - 3D XPoint Storage Tech Reaches Its End

by Ryan Smith on July 28, 2022 5:00 PM EST

Posted in Storage | Intel | 3D XPoint | Optane | Optane Memory

Intel Kills Optane Memory Business, Pays $559 Million Inventory Write-Off

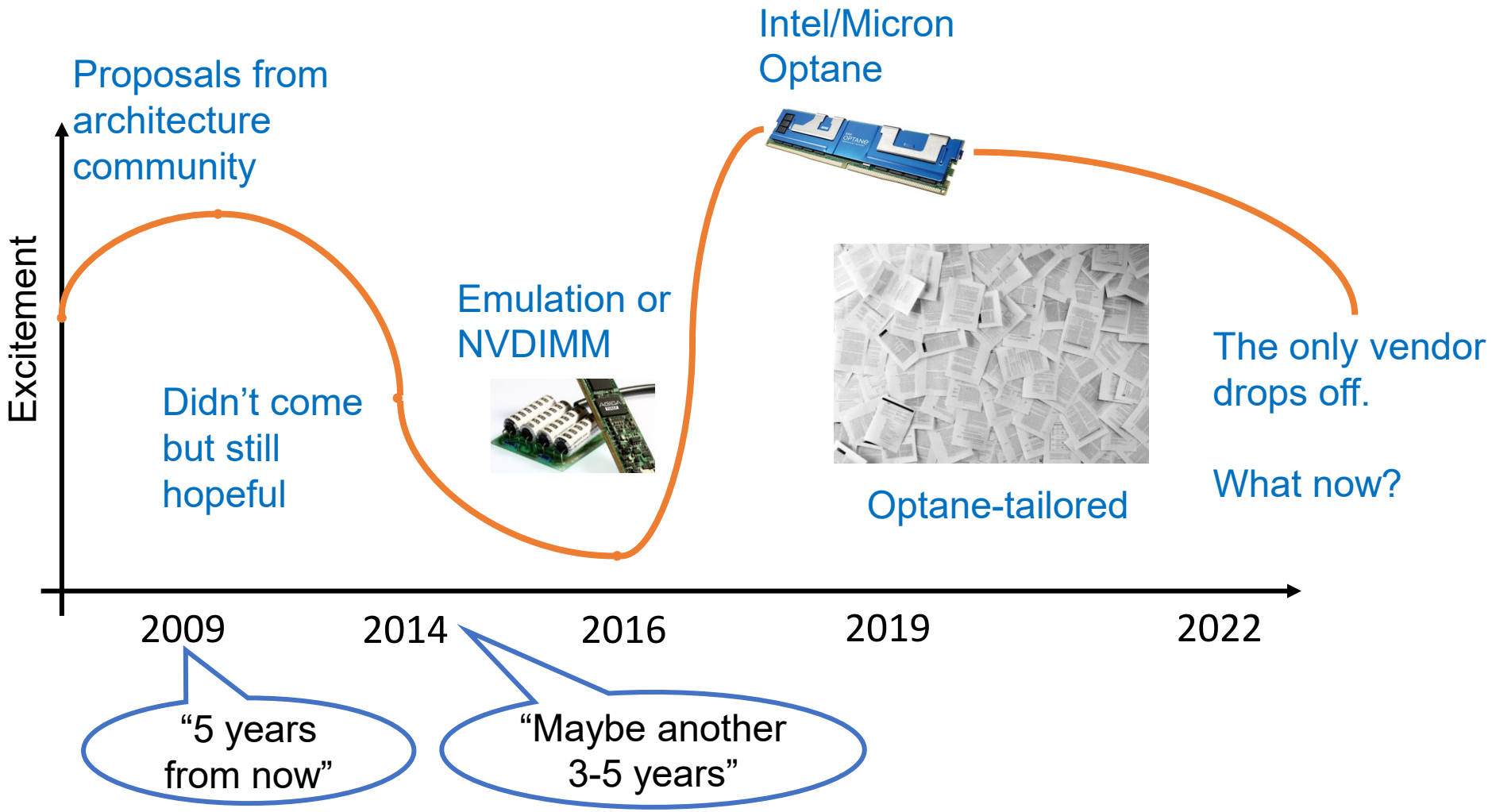
By Paul Alcorn published July 28, 2022

3D XPoint at the last crossroad.

Not the first time

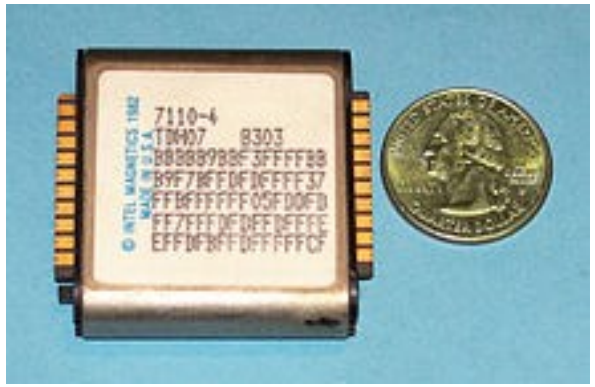
* https://www.techtarget.com/searchstorage/news/252523339/Intel-pulls-the-plug-on-Optane
* https://www.anandtech.com/show/17515/intel-to-wind-down-optane-memory-business
* https://www.tomshardware.com/news/intel-kills-optane-memory-business-for-good

Recent Timeline



Another Bubble Memory [32] (1960-1981)?

- Was the hope, like today's PM [31]
- Did not make it due to
  - Scalability/price
  - Complex to make
  - Require memory controller help
  - DRAM and magnetic disks caught up
- Optane with similar issues
  - Performance per $: lower than SSDs [33]
  - SSDs getting faster and faster
  - More complex memory controller
  - Single vendor



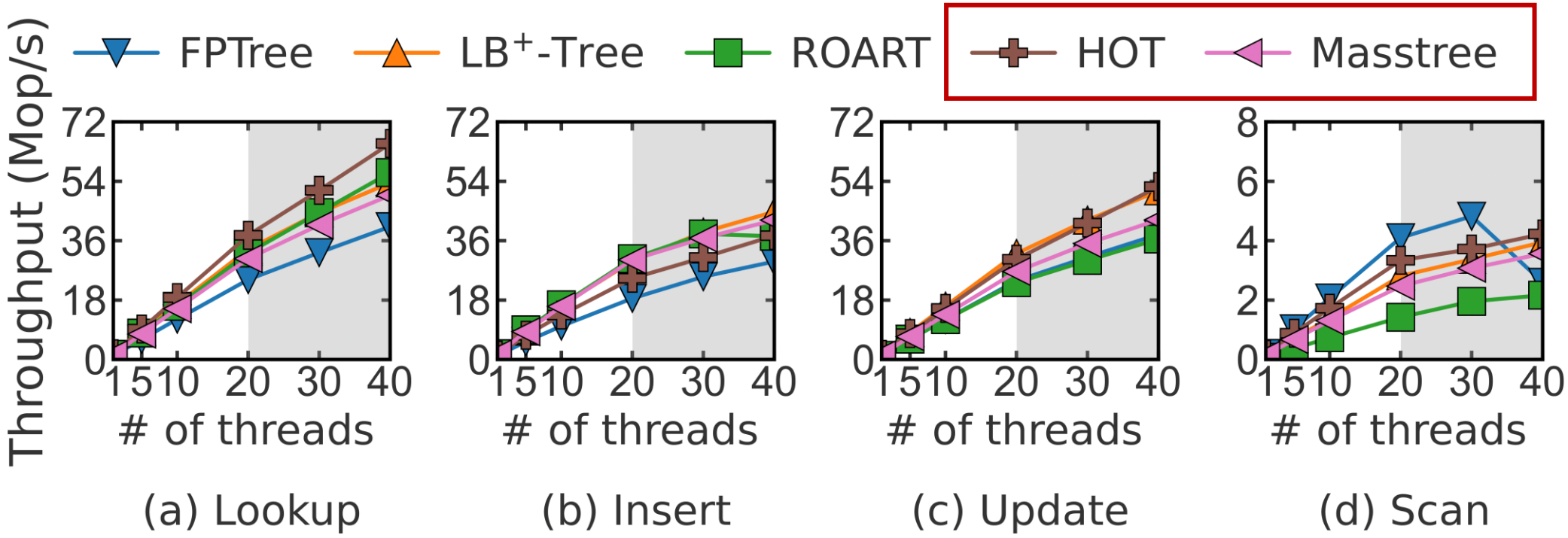
Intel (!) 7110 bubble memory*

Relevance of today's software techniques for PM?

* https://en.wikipedia.org/wiki/Bubble_memory#/media/File:Bubble_memory_module.jpg

Potential: PM Techniques on DRAM [26]

- Running PM range indexes on DRAM
  - No extra flushes/fences, using DRAM allocator



1. PM index techniques also effective for DRAM
2. Should focus more on full functionality [26]

Future: a Storage Jungle [33]

- NVDIMMs
  - Always been there
- Carbon Nanotubes: WIP
- Optane PMem
- Storage
  - Faster flash memory/SSDs
  - SSDs with memory semantics
  - 3D-stack DRAM
  - CXL enabling pooled memory

Thank you! + Q&A

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